

Project code: 4PD0FN010001
PCB P/N: TBD
PCB No. : 17910
Revision: A00


Pinehill 13.3" Schematics

Kaby lake-R

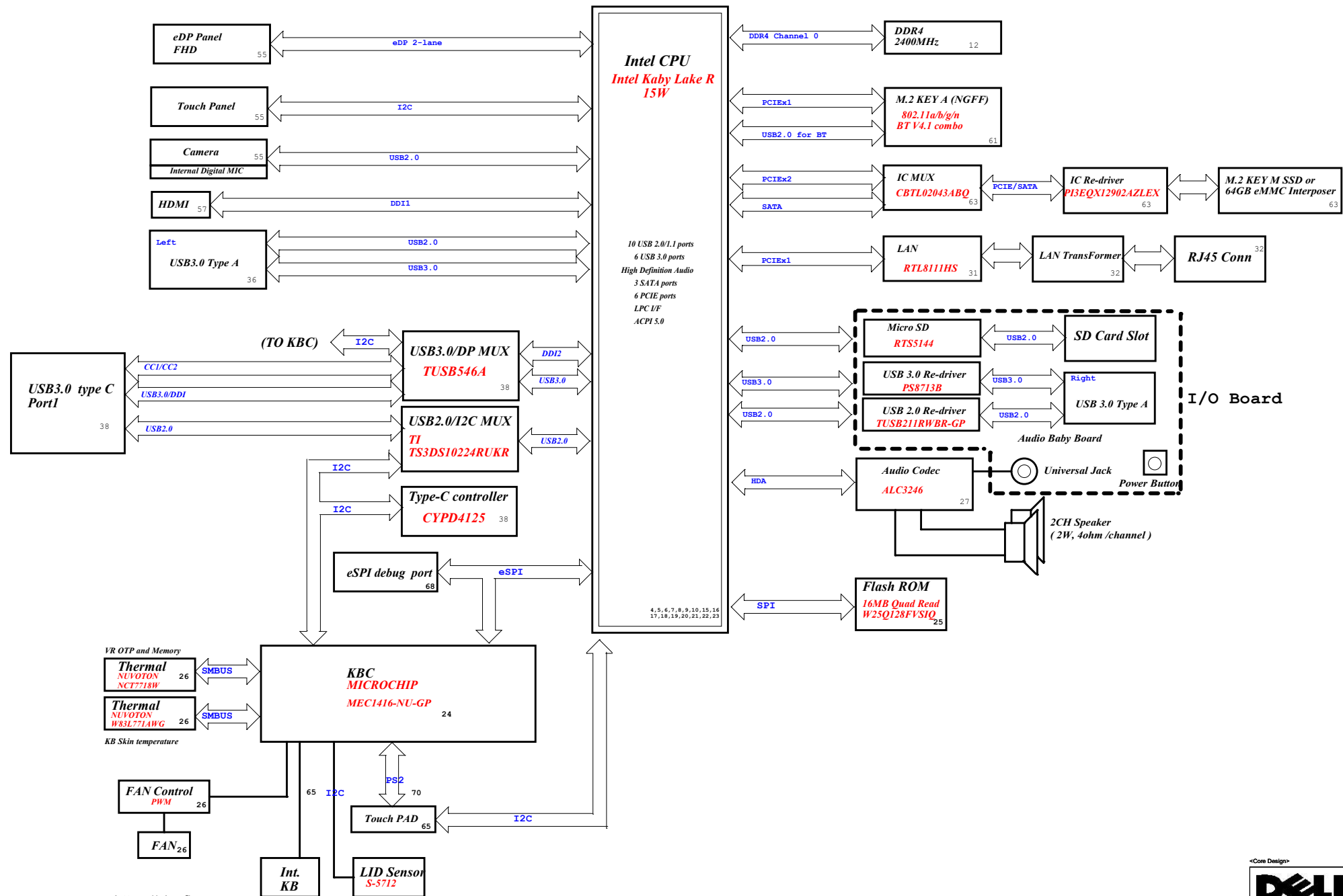
2018-09-20
REV : A00

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Title		
Cover Page		
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PINEHILLS-KBL-R 13.3" Block Diagram



CHARGER	
ISL88738HRTZ	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
RT6575DGQW	45
INPUTS	OUTPUTS
DCBATOUT	PWR 5V 5V S5 5V AUX S5 PWR 3D3V 3D3V S5
CPU Core Power	
ISL95859AHRTZ	
CSD97396Q4M	
CSD97396Q4M	
ISL95808HRZ-T-1	46-50
INPUTS	OUTPUTS
DCBATOUT	VCC CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCSA
DDR4	
RT8231AGQW	51
INPUTS	OUTPUTS
DCBATOUT	1D2V S3 0D6V S0
CPU DCDC-V1D00A	
AOZ2262QI-10	52
INPUTS	OUTPUTS
DCBATOUT	1D0V S5
LDO-V1D8V	
AOZ2023PI-GP	54
INPUTS	OUTPUTS
3D3V S5	1D8V S5
LDO-V2D5V	
AOZ2023PI-GP	54
INPUTS	OUTPUTS
3D3V S5	2D5V S3
5V/3V S0	
G5016KD1U	40
INPUTS	OUTPUTS
5V S5	5V S0
3D3V S5	3D3V S0
VCCSTG	
SLG59M1470VTR	40
INPUTS	OUTPUTS
1D0V S5	+VCCSTG
VCCST	
AP8939GN3-GP	40
INPUTS	OUTPUTS
1D0V S5	+V1.000_CPU


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Main Func = CPU

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Main Func = CPU

24	PECI	《 》
24,44,46	PROCHOT#_CPU	《 》
24,65	TP_WAKE_KBC#	《 》
24,55	TOUCH_PANEL_INTR	《 》
55	TOUCH_PANEL_PD#	《 》

XDP

```

99      XDP_BPM1          <<>>=====
99      XDP_BPM0          <<>>=====

99      PCH_JTAG_TDO     <<<<=====
99      PCH_JTAG_TDI     <<<<=====

99      PCH_JTAG_TMS     >>>>=====
99      PCH_JTAG_TCK     >>>>=====


99      XDP_TRST#        >>>>=====
99      XDP_TCK_JTAGX    >>>>=====

```

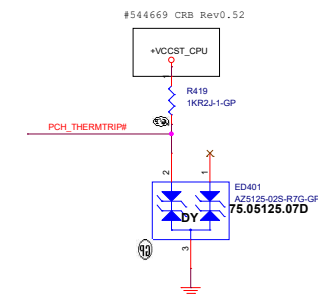
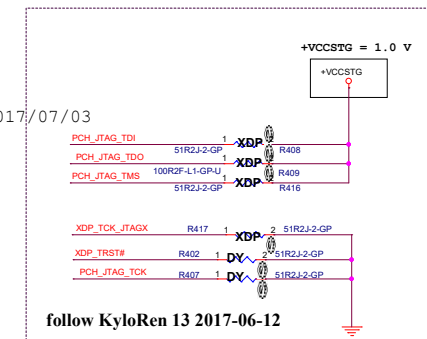
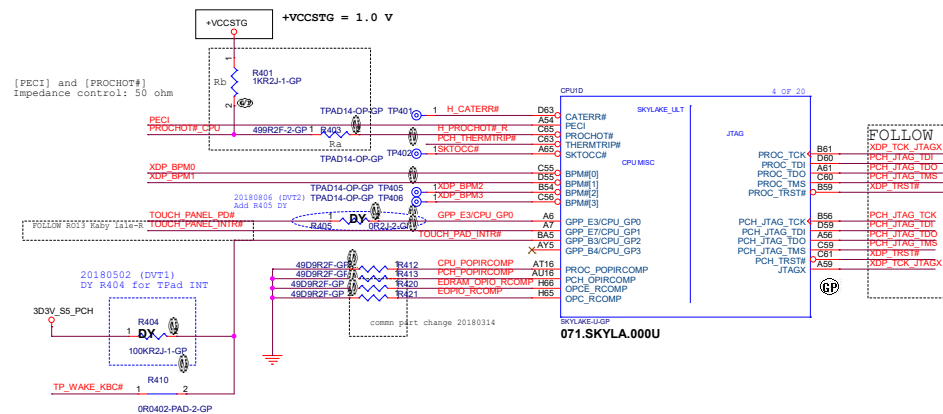
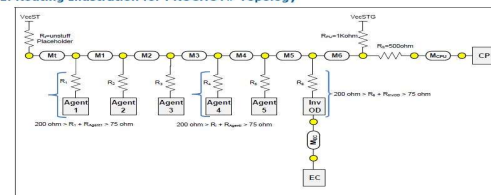
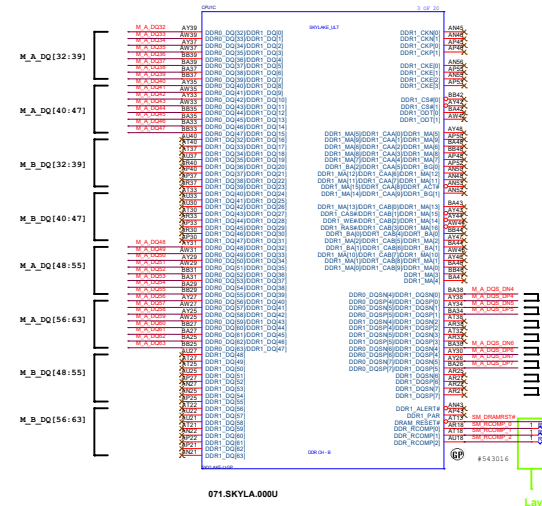
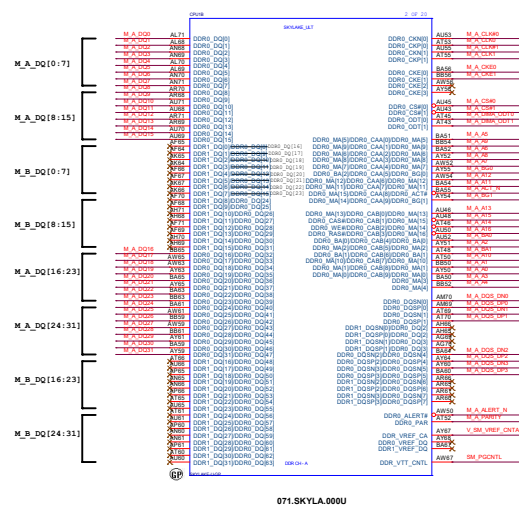
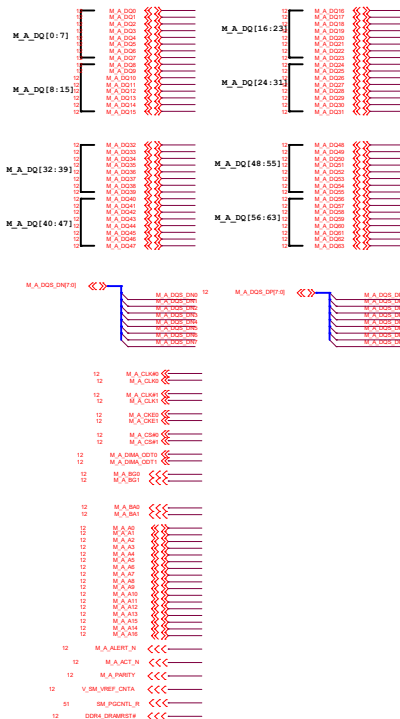


Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches



Design Guideline:
SM_RCOMP keep routing length less than 500 mils

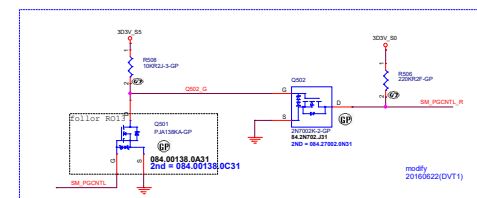
DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT
4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

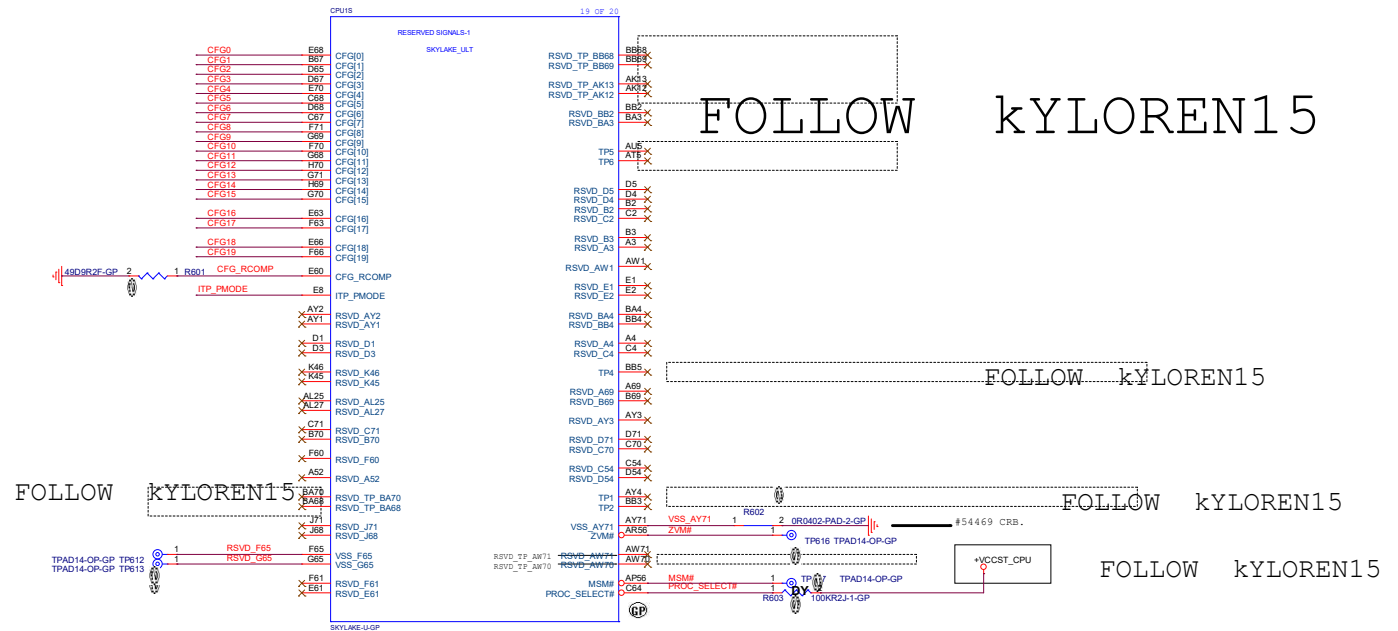
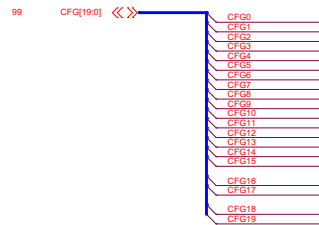
Table 4-41. ODT Signals Connectivity table

[illegible]

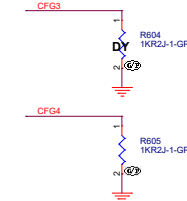
	DPDR3	DDR4 (ECC)
Notes:		
1.	For additional ODT signal connection details reference the Customer Reference Board (CRB) schematic and board file (RVP3 - SKU-V LPDDR3, RVP4 - SKU-U LPDDR3)	
2.	LPDDR3 RVP4 ODT is always disabled by BIOS/MMIO. ODT signal is controlling only RVP4 ODT.	
3.	DDR4L ODT input is held high (ACTIVE). RTT NOM is defined by BIOS as High-Z in both banks, when a RAS receives write command it enables RTT RV (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z)	
4.	These guidelines are related to DDR4L supported Memory down topologies only. 2R x16 DOP single side 2R x16 DOP dual sided and 2Rx8 dual side.	



Layout Note:



PCH strap pin:

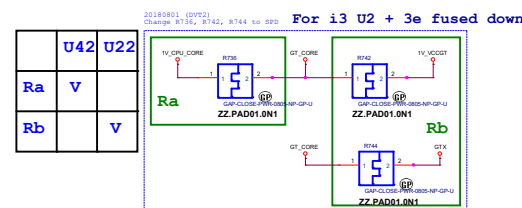
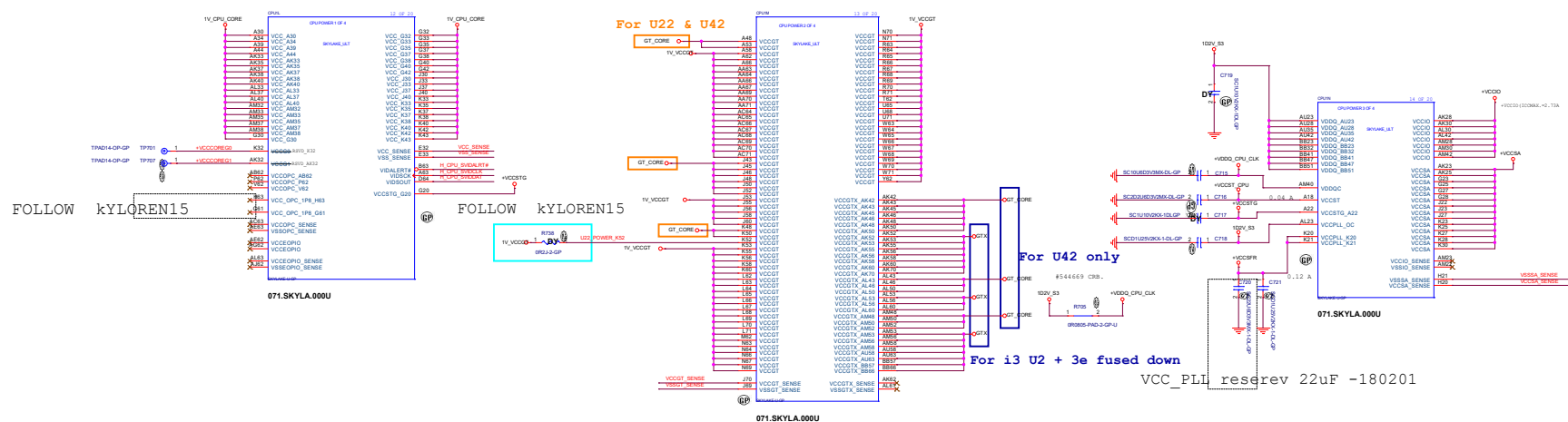


071.SKYLA.000U	
[BDW Only] PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED
(#543016)	
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

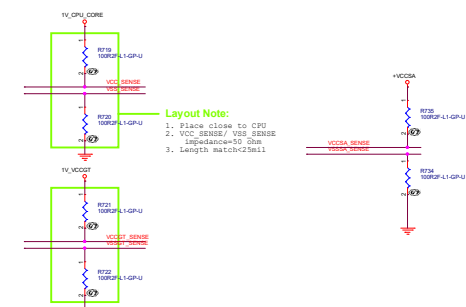
SKL (#543016) :

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

40	VSSA_SENSE	<<<	_____
40	VCCA_SENSE	<<<	_____
40	VCC_SENSE	<<<	_____
40	VSS_SENSE	<<<	_____
40	VCGT_SENSE	<<<	_____
40	VSSGT_SENSE	<<<	_____
40	SVD_CLK_CPU	<<<<	_____
40	SVD_DATA_CPU	<<<<	_____
40	SVD_ALERT#_CPU	<<<	_____



*After Gerber out need to tell PSE which location need open stencil, Which close stencil

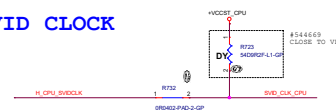


SVID DATA

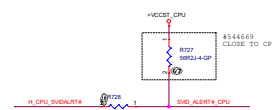
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK



SVID ALERT



SVID 543016:

Figure 10-7. Routing Illustration for SVID Topology

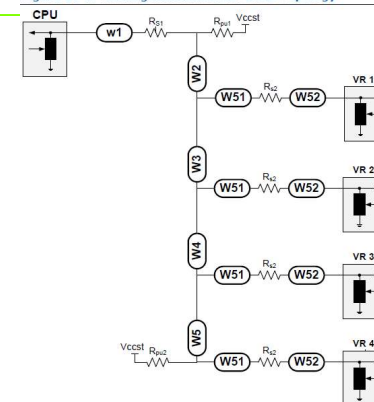
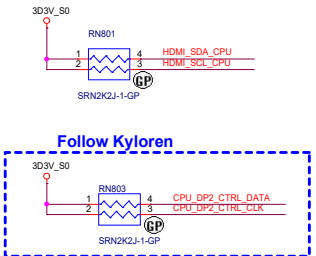
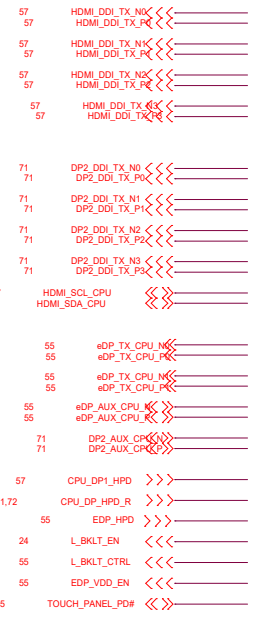


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R ₅₀₁ [°]	R ₅₀₂ [°]	R ₅₁ [°]	R ₅₂ [°]	VCC [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.8
VIDSKC							Empty	45	0	50	
VIDALERT #							56	Empt. Y	220	0	

Main Func = CPU



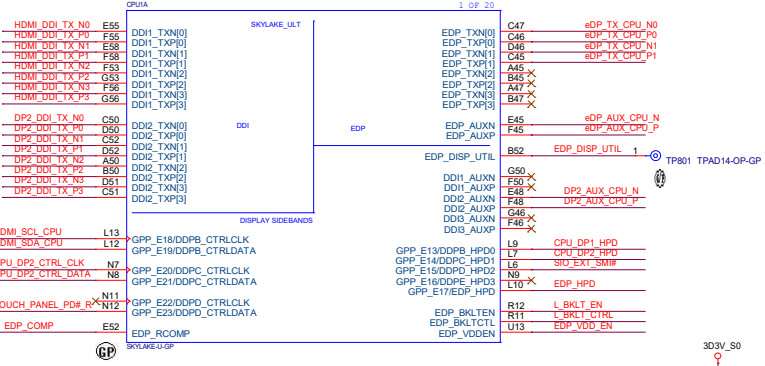
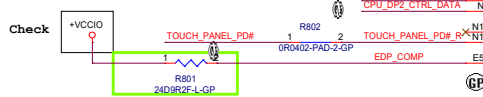
Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. 1 = Port C is detected.

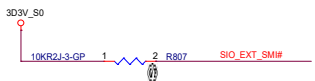
These two signals have weak internal pull-down.

HDMI
DP for Type-C Mux

HDMI



for Type-C Mux



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

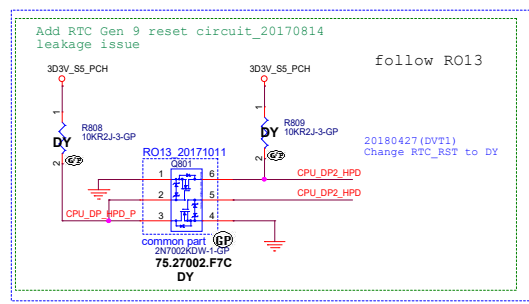
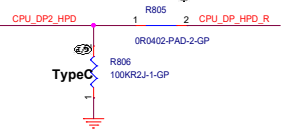
(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω resistor.

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

DP for Type-C Mux



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File # CPU_(DDI/EDP)


Side # Custom Document Number: Pinehill-KBL-R Rev A00

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Main Func = CPU

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Main Func = CPU

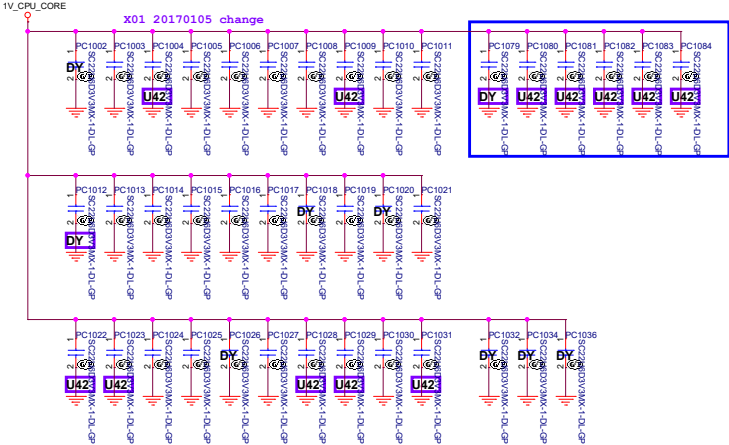
follow KYLOREN 15" 20170705

VCC_CORE

U-line 22 15W
IccMax current=10ms max = 31 A

22U 0603 x 30 (3DY)

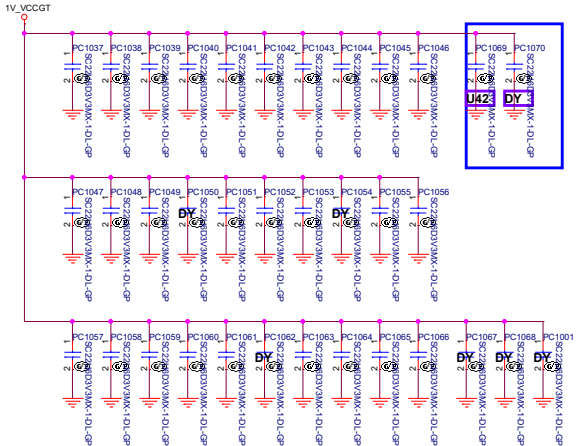
20180611 (DVT1)
DY PC1020, PC1018, PC1026, PC1079, PC1002,
PC1012, PC1050, PC1062, PC1070, PC1054
by power Team



VCCGT

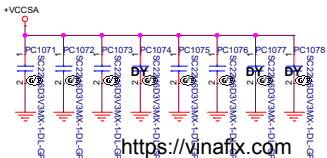
U-line 22 15W
IccMax current=10ms max[A] = 64 A

22U 0603 x 30 (3 DY)



VCCSA

22U 0603 x 8 (3DY)



https://vinafx.com

Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V) ¹	
VCCGT		8x 10uF 0402	Place on secondary side, underneath the package
	10x 10uF 0402		
	12x 1uF 0201		
		3x 47uF 0805 (6.3V) ¹	
VCCGTx		7x 22uF 0603	Place as close to the package as possible
		3x 47uF 0805	
		5x 22uF 0603	
VCCSA	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	
	7x 10uF 0402		
	7x 1uF 0201		
VCCIO	6x 10uF 0402		Place on secondary side, underneath the package
	2x 10uF 0402		
	4x 1uF 0201		
		4x 1uF 0402	
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

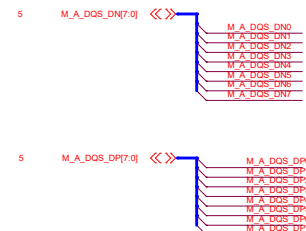
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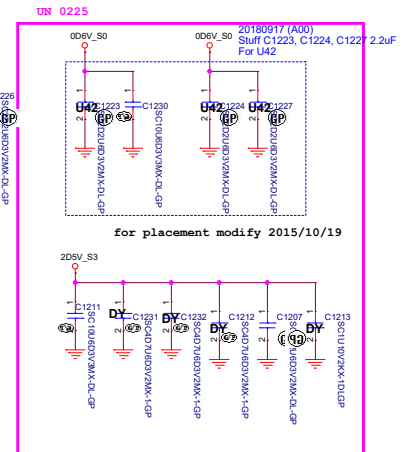
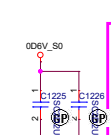
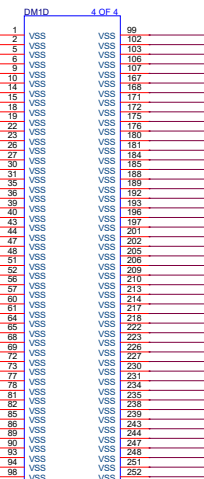
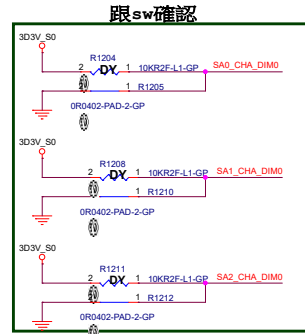
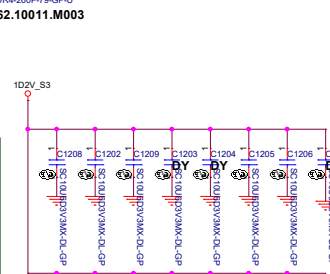
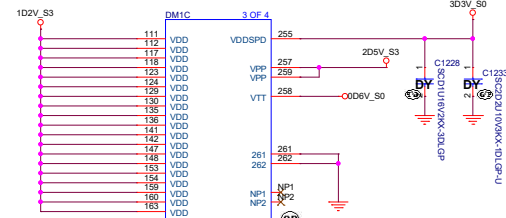
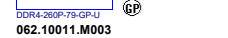
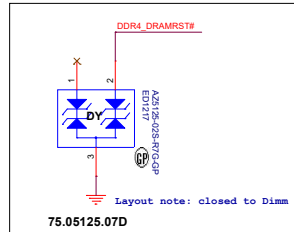
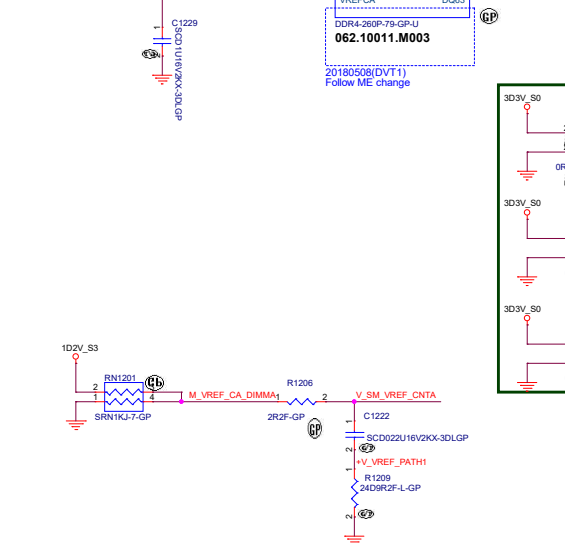
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Taippei Hsien 221, Taiwan, R.O.C.

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CPU (Power CAP1)		
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A2	Kyloren 15" KBL-U	A00
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Main Func = MEMORY



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Title			
DDR4-SODIMM1			
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Main Func = MEMORY

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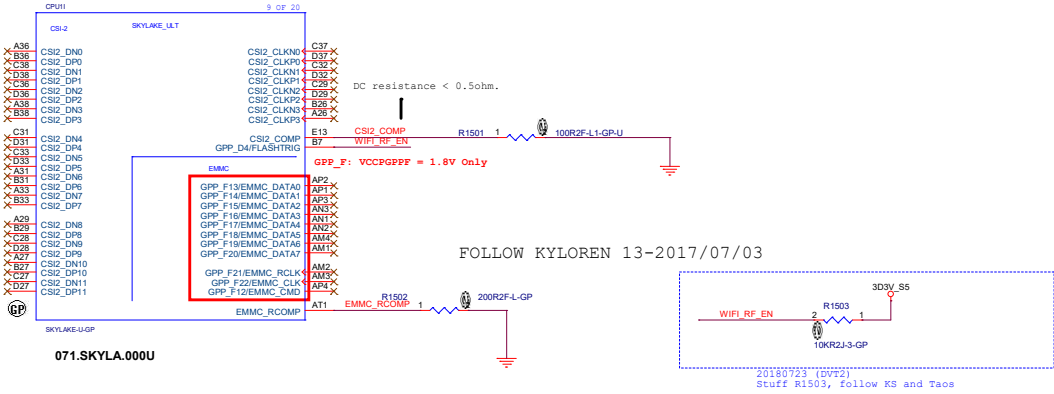
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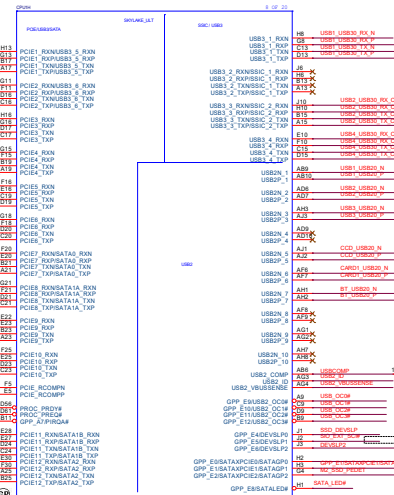
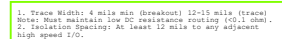
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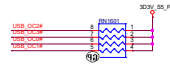


[#545659 Rev0.7]
GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



WLAN



The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3.3.

Platform		Project	
SKU			Tulip
Can1	US82 Port2		USB 3 (1/0) Port
Can2	US83 Port2	SSIC1	NC
Can3	US83 Port2	SSIC2	NC
Can4	US83 Port2		NC
Can5	US83 Port2	PCie Port1	NC
Can6	US83 Port8	PCie Port2	gGPU
Can7	PCie Port5	QSE	NC
Can8	PCie Port6	QSE	NC
Can9	PCie Port7	QSE	WLAN
Can10	PCie Port8		NC
Can11	PCie Port9	SATA0	Hard
Can12	PCie Port10	SATA1	ODD
Can13	PCie Port9	QSE	NC
Can14	PCie Port10	QSE	NC
Can15	PCie Port11	SATA1	NC
Can16	PCie Port12	SATA2	NC
Can17			USB 3 (1/0) Port
US82 Port1			USB 2 Port
US82 Port2			USB 2 Port 3
US83 Port3			NC
US82 Port3			Camera
US82 Port7			WLAN
US82 Port8			Touch Panel
US82 Port9			Card Reader
US82 Port10			NC
US82 Port11			NC
US82 Port12			NC

TBD

2018/03/05
Port mapping for PINEHILLS

PCIe Table			USB 2.0 Table		USB 3.0 Table	
Port	Device	Share BUS	Pair	Device	Pair	Device
1	N/A	USB3_0_5	0	Type-C	1	Type-C
2	N/A	USB3_0_6	1	USB3.0 MB	2	WWAN
3	N/A		2	USB3.0 DB	3	USB3.0 MB
4	N/A		3	WWAN	4	USB3.0 DB
5	N/A		4	CAMERA		
6	WLAN		5	Card Reader		
7	SSD	SATA0	6	WLAN (BT)		
8	WWAN		7	Touch Panel		

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

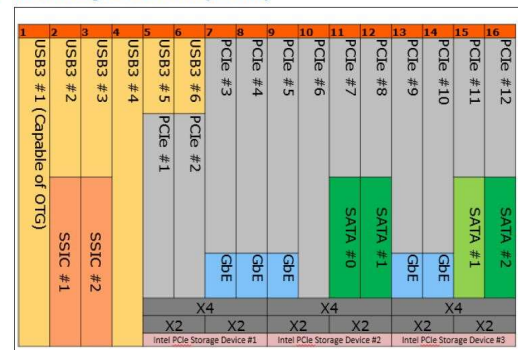


Table 24-2. PCI Express* Port Feature Details

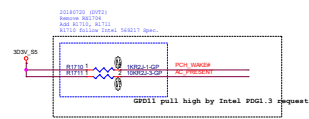
SKL	Max Device (Ports)	Max Lanes	PCIe® Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	4x1	Port1		Port2		Port3		Port4		Port5		Port6	
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	4x1	Port1		Port2		Port3		Port4		Port5		Port6	
	1x2									Port9			
	2x1									Port9		Port10	

Main Func = PCH

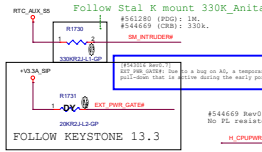
24.00	RUNPWROK	>>>
24.25.40.00	3V_SV_PCH	>>>
24.00	SYS_PWROK	>>>
90	H_VCCST_PWROK	>>>
31	PCH_LAN_WAKEUP	>>>
61	PCH_WLAN_WAKEUP	>>>
24	LAN_WAKEUP	>>>
31.01.03.00	PLT_RST#	<<<
24	PCH_RESET#	<<<
17.00.00	PM_RESET#	<<<
90	KDP_RESET#	<<<
34.00	WIC_POWERDOWN	<<<
24.00	SDO_POWERDOWN	<<<
43.41	AC_R#	<<<
10.01	WFI_RF_EN	<<<
50	3V3_CAM_EN	<<<
24.01	ALX_EN_WOHL	<<<
24.00	RESET_OUT#	<<<
40.00.00	SDO_SLP_S#	<<<
30.27.00	PM_SLP_S#	<<<
40.04	PCH_WAKER	<<<



Follow Kyloren

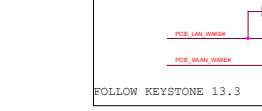


FOLLOW Kyloren13

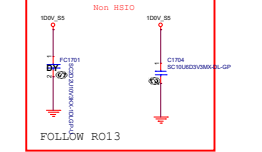


FOLLOW KEYSTONE 13.3

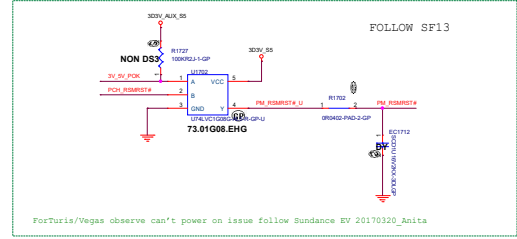
Follow Santa Fe 13.3"/14"



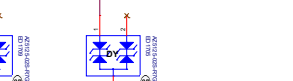
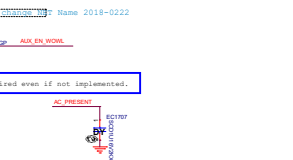
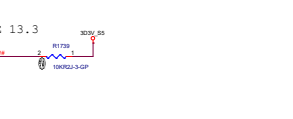
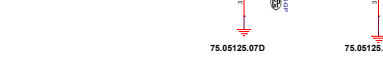
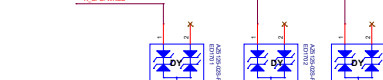
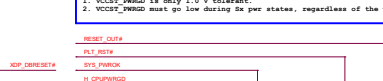
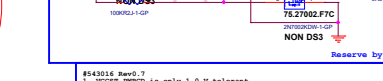
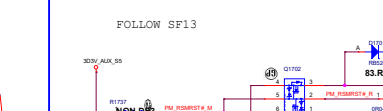
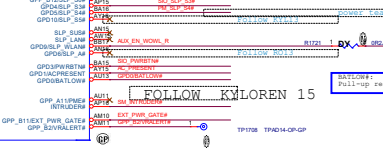
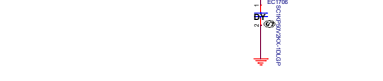
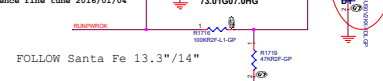
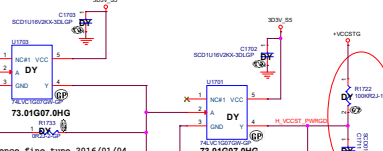
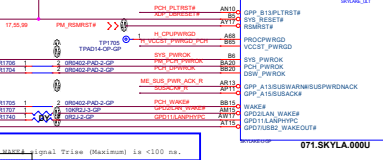
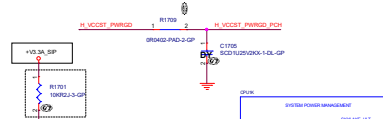
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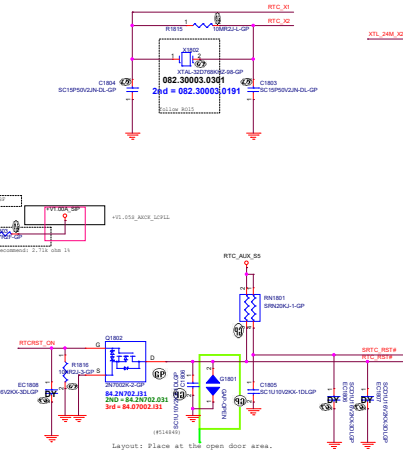
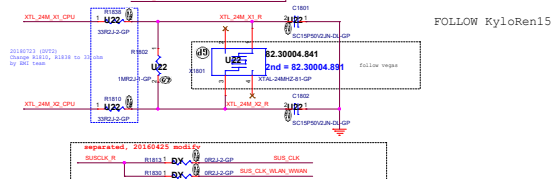
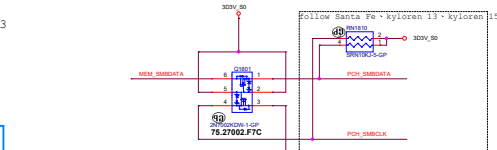
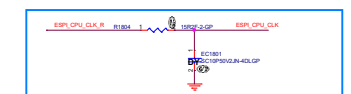
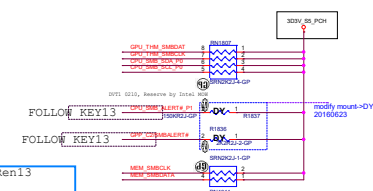
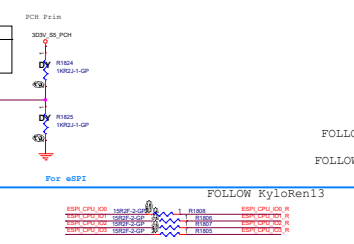
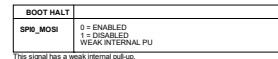
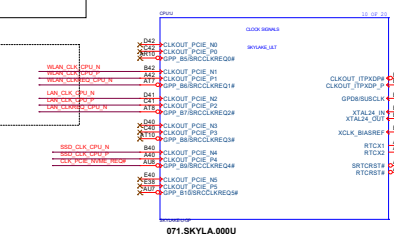
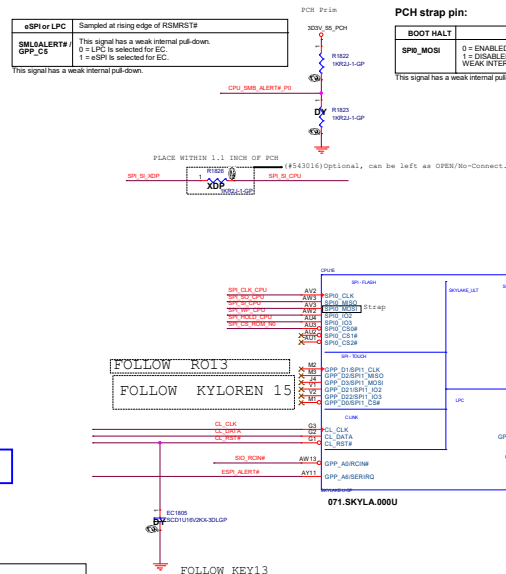
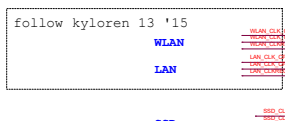
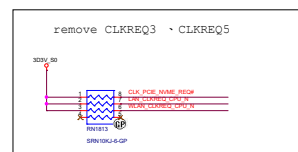
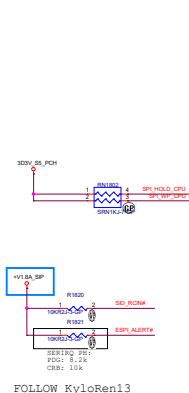


ME_SLP_PWR_ACK_R



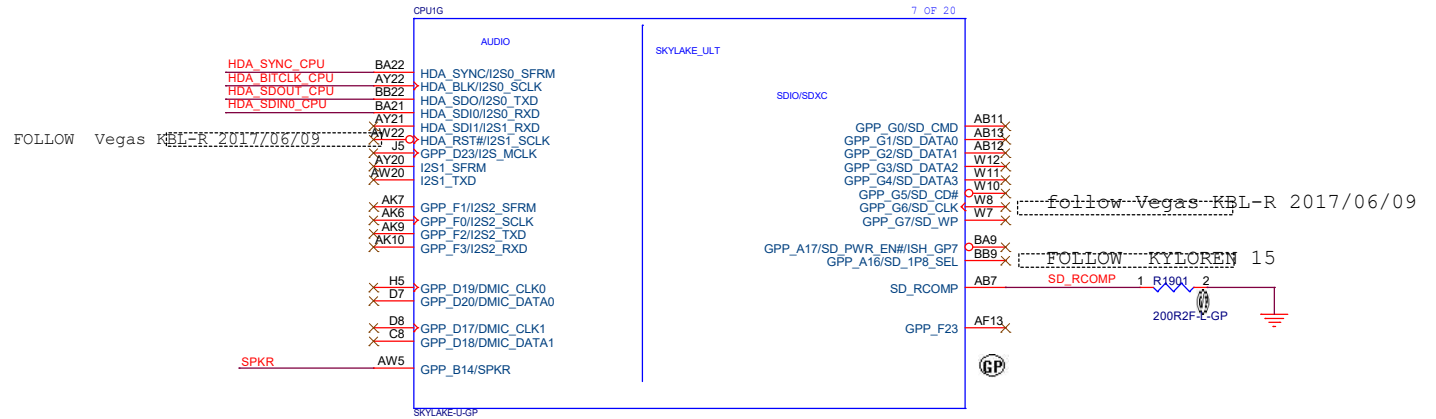
ForTuris/Vegas observe can't power on issue follow Sundance EV 20170320_Anita





Main Func = PCH

27 HDA_SDIO_CPU >>> _____
 27 SPKR <<< _____
 27 HDA_SYNC_CODECC <<< _____
 27 HDA_BITCLK_CODECC <<< _____
 27 HDA_SDOUT_CODECC <<< _____
 98 ME_FWP_R >>> _____



PCH strap pin:

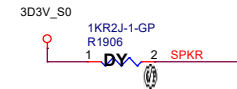
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

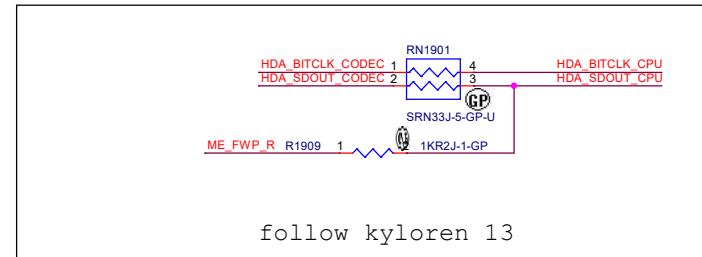
PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



HDA_SYNC_CODECC R1908 1 2 0R0402-PAD-2-GP HDA_SYNC_CPU

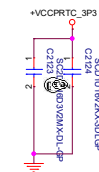
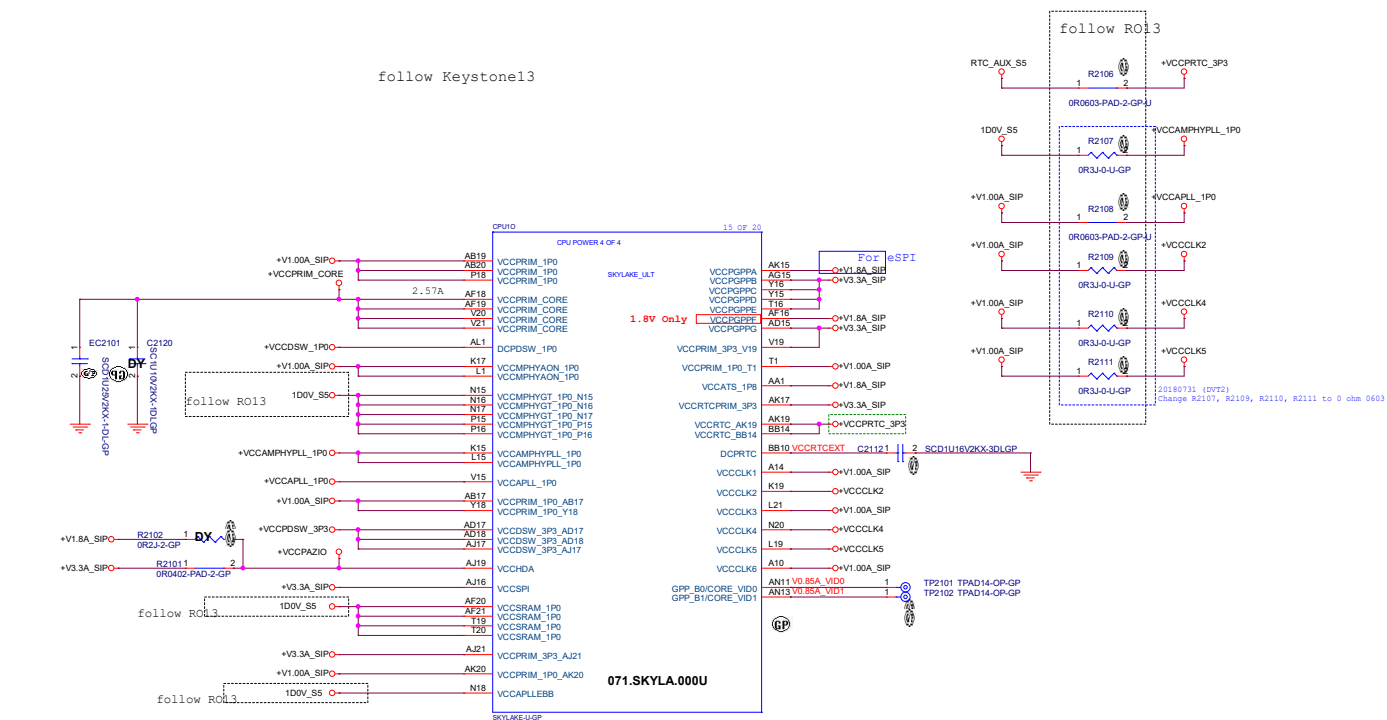


follow kyloren 13

<Core Design>

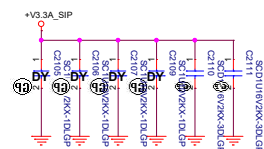
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

PCH (HDA/SDIO/SDXC)	
Size A3	Document Number
Pinehill-KBL-R	
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Layout Note:

```
0.1uF:
C2124 near AK19
1uF:
C2123 near Ak19
```

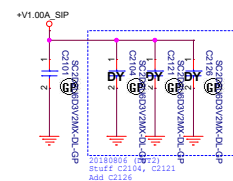
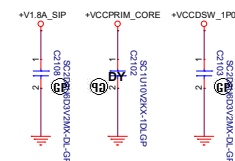


Layout Note:

```

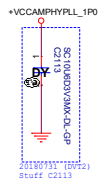
1uF:
C2105 near V
C2106 near A
C2107 near A
C2109 near Y
C2110 near T

```



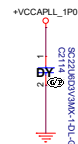
Layout Note:

```
1uF:
C2101 near A
C2104 near F
C2121 near A
C2126 near A
```



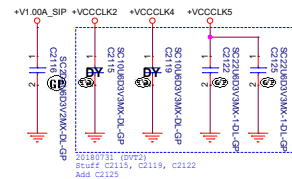
Layout Note:

22uF:
C2113 near K1



Layout Note:

22uF:
C2114 near V



Layout Note:

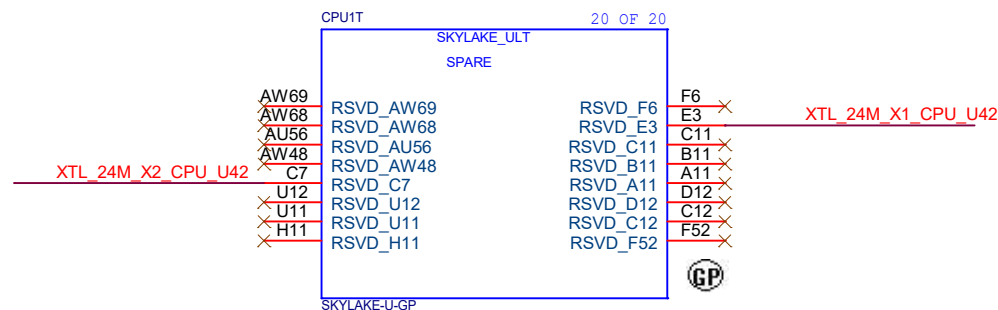
```

1uF:
C2116 near A
22uF:
C2115 near F
C2119 near M
C2122 near I
C2125 near I

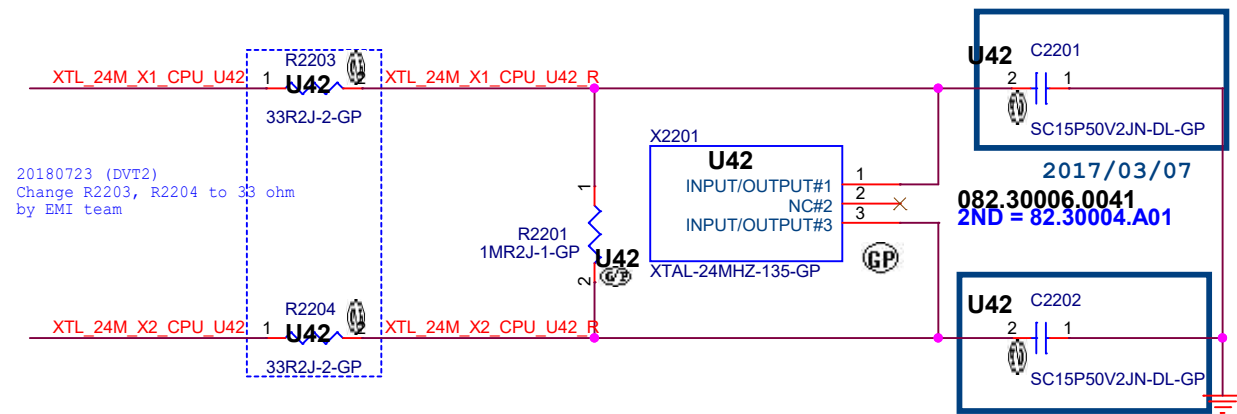
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Main Func = PCH


follow Kyloren13



071.SKYLA.000U

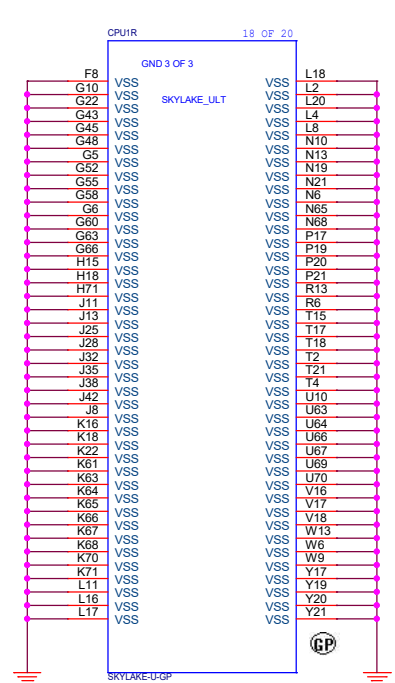
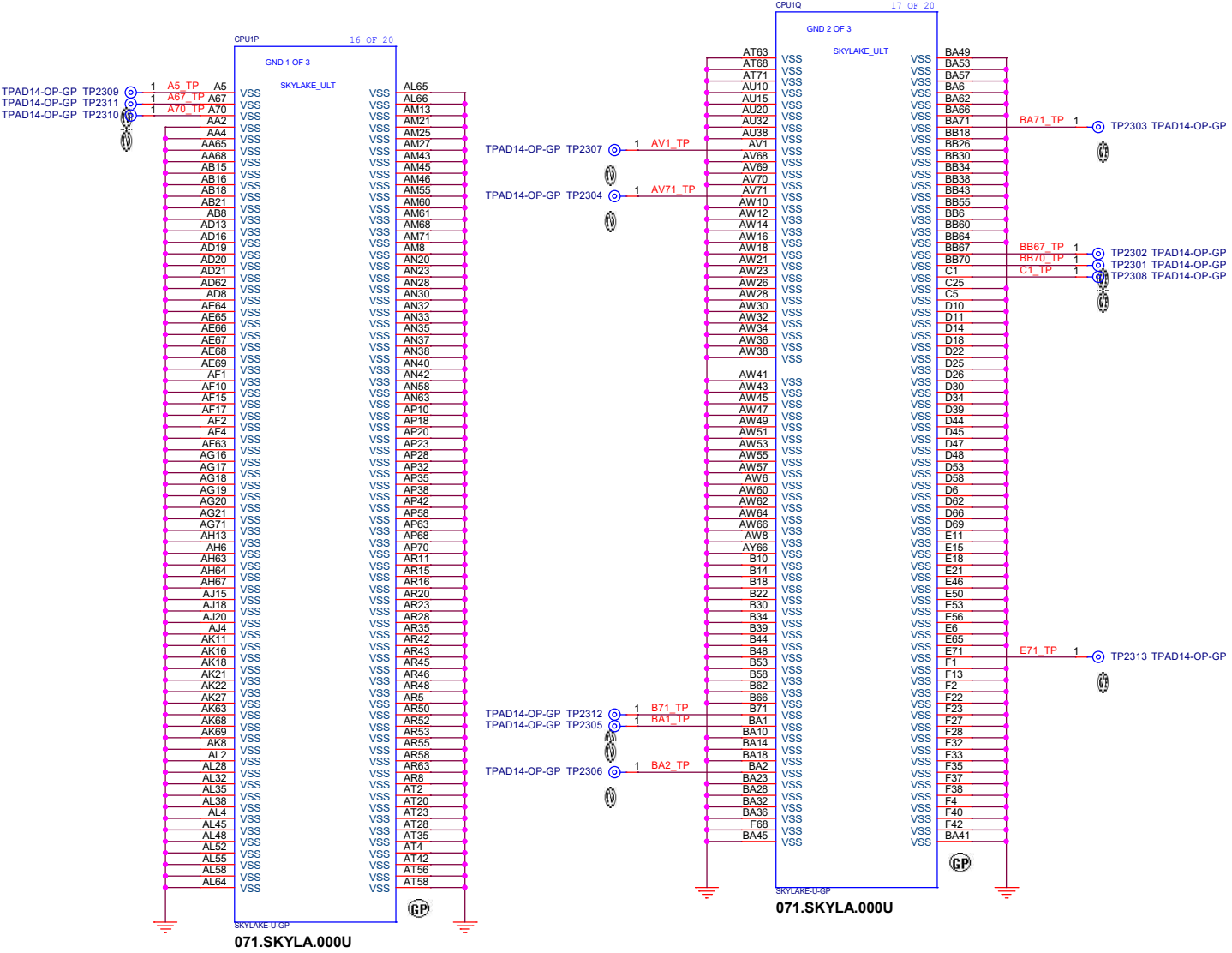


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 022_PCH_(SPARE)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 22 of 106	

Main Func = PCH

follow KYLOREN 13




071.SKYLA.000U

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>



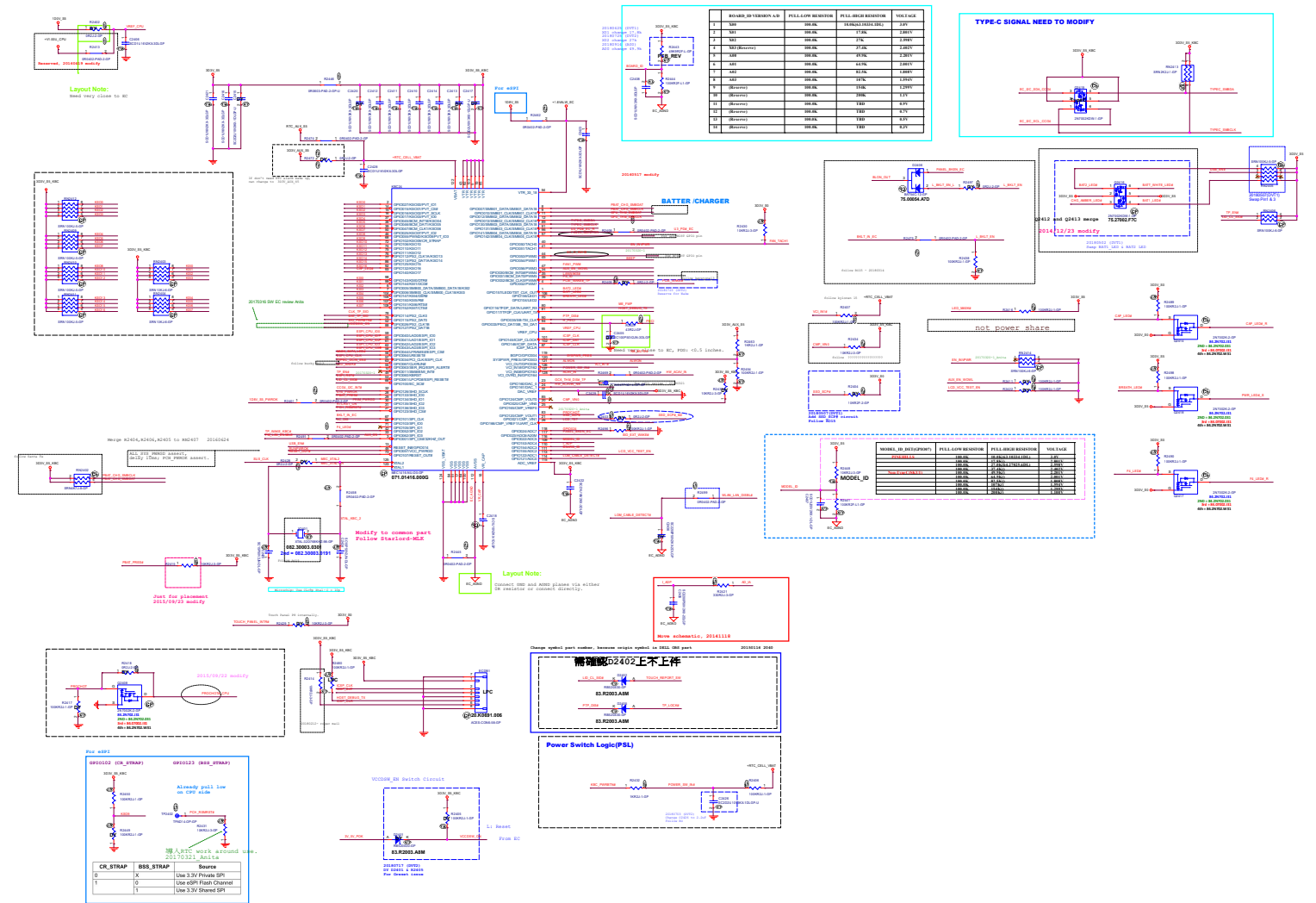
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Taipei Hsien 221, Taiwan, R.O.C.

Title

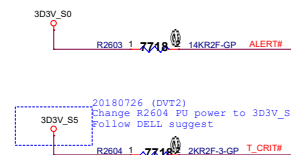
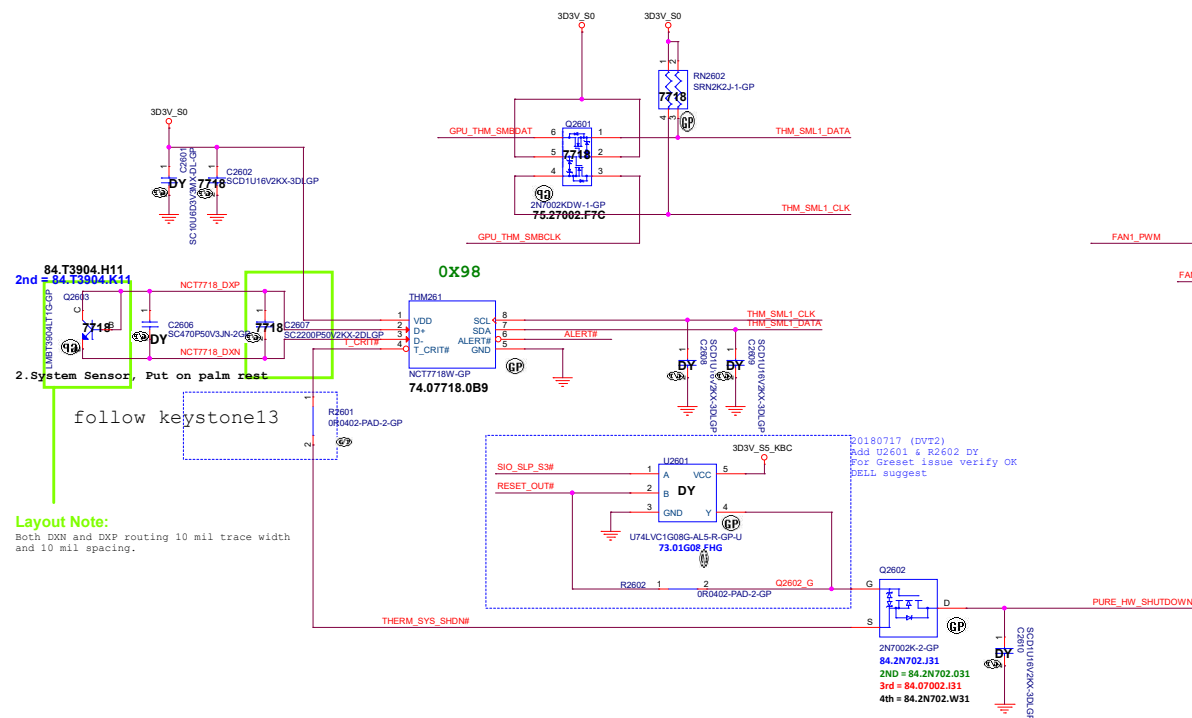
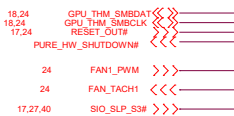
PCH (VSS)

Size A3 Document Number **Pinehill-KBL-R** Rev **A00**

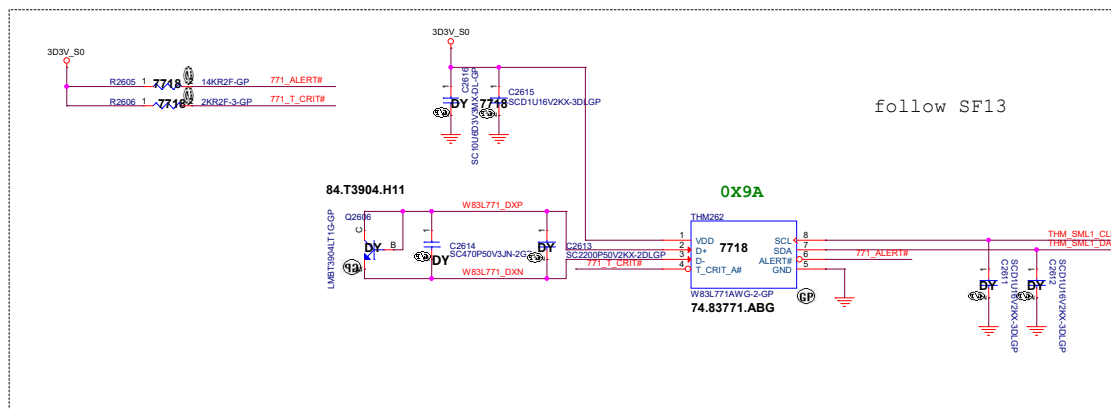
Date: Wednesday, September 26, 2018 Sheet 23 of 106



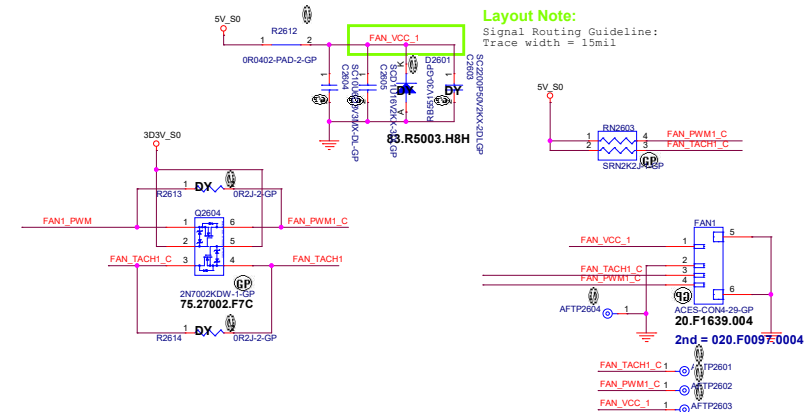
Main Func = Thermal Sensor



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



PWM FAN1



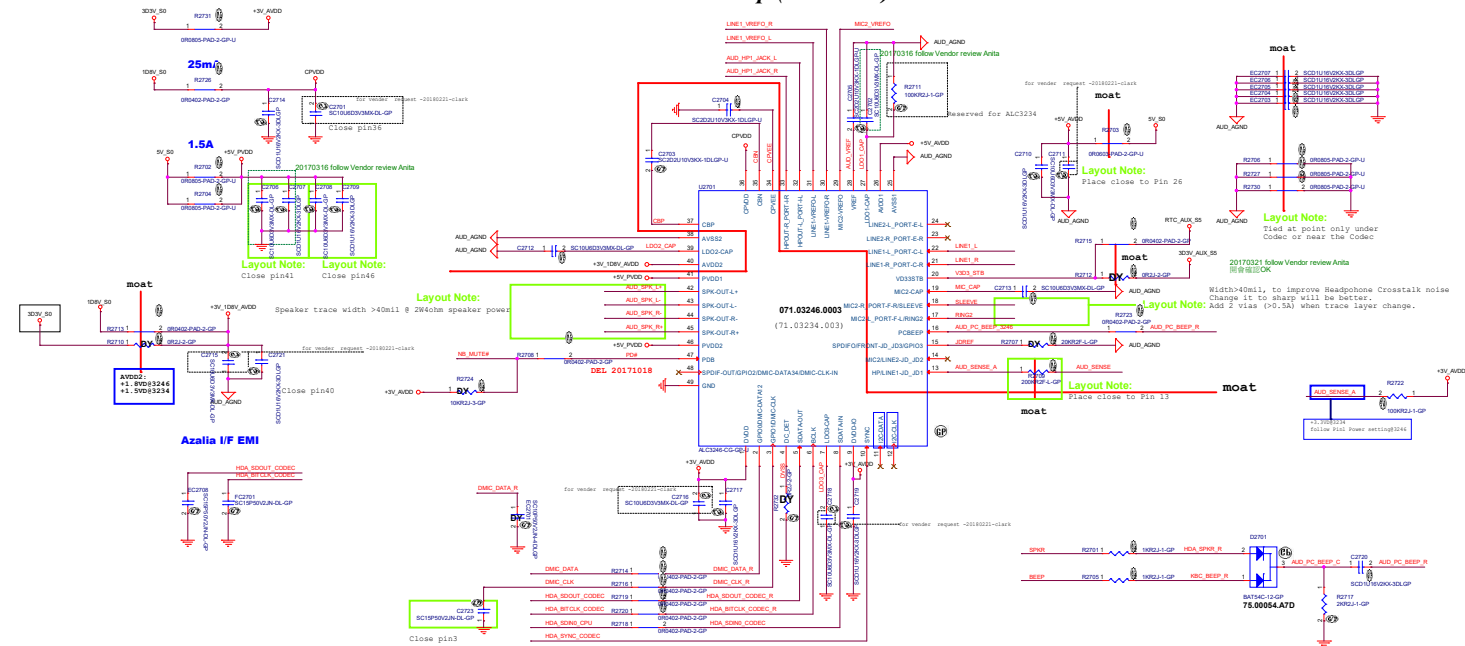
<https://vinafix.com>

```

20 LINE1_VREF0_R <<<
21 LINE1_VREF0_I <<<
22 AUD_HPL_JACK_L <<<
23 AUD_HPL_JACK_L <<<
24 NR_BUFFER >>>
25 DMC_DATA >>>
19 HDA_SCOUT_CODEC <<<
18 HDA_BTCLK_CODEC <<<
17 HDA_SONG_CPU <<<
16 HDA_SONG_CODEC <<<
55 DMC_CLK <<<
19 SPW01 <<<
24 BEEP >>>
17,26,40 SEQ_SLIP_S3W >>>
20 MIC2_VREF0 <<<
29 LINE1_L <<<
29 LINE1_R <<<
20 AUD_SENSE >>>
26,65 SLEEVE >>>
26,65 RWNG2 >>>
29 AUD_SPK_L+ <<<
29 AUD_SPK_L- <<<
29 AUD_SPK_R+ <<<
29 AUD_SPK_R- <<<

```

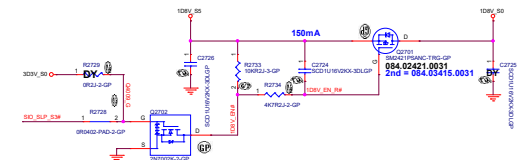
Audio Codec Chip (ALC3246)



Power requirement:

DVDD must \geq DVDD_IO,


+3.3V 1.8V DVDD	+3.3V 1.8V DVDD IO	Result
3.3V/+10%	3.3V/+10%	support
3.3V/+10%	1.8V/+5%	support
1.8V/+5%	1.8V/+5%	support
1.8V/+5%	1.5V/+5%	support
1.8V/+5%	3.3V/+10%	Not support



Main Func = PCH

(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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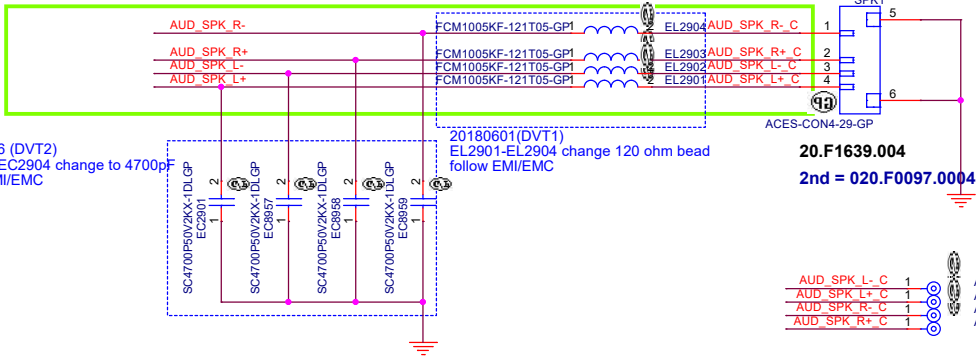
Main Func = Audio

follow SF13

Speaker

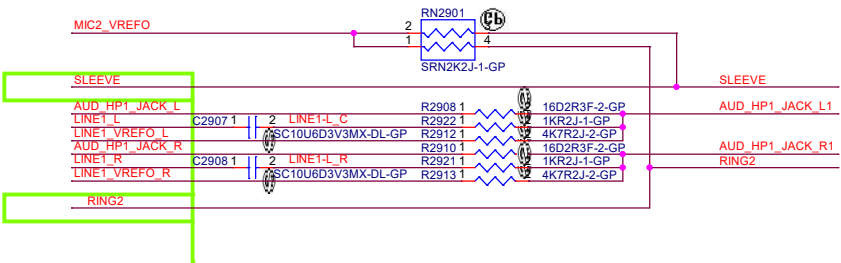
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



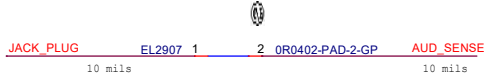
CONN Pin	Net name
Pin1	SPK_R-
Pin2	SPK_R+
Pin3	SPK_L-
Pin4	SPK_L+

Universal Jack (Moved to I/O Board)



Layout Note:

Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.



Main Func = Audio

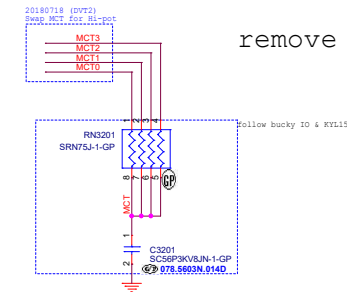
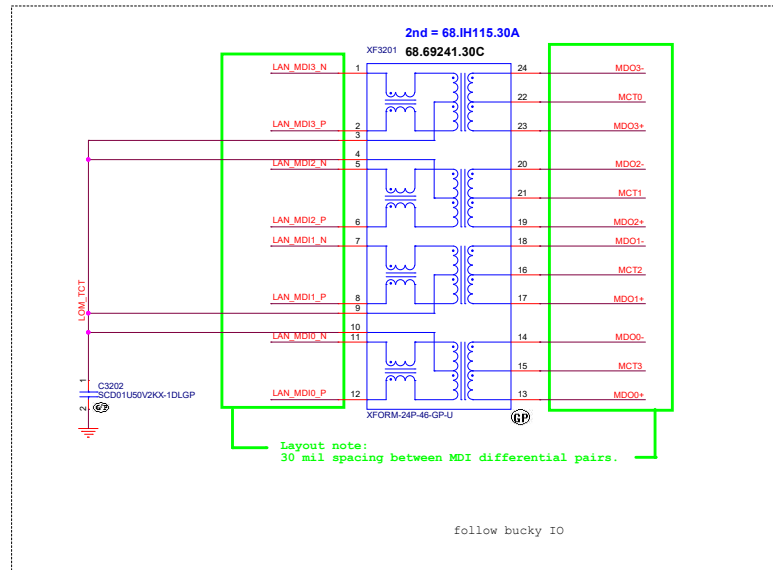
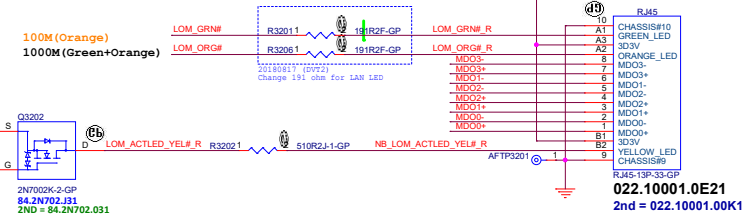
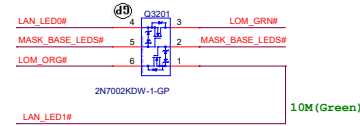
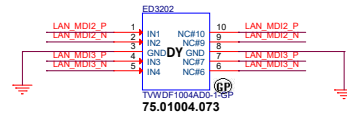
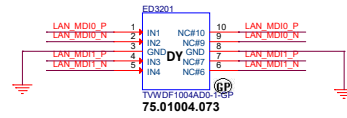
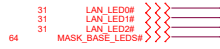
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Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 30 of	106

LAN TransFormer


follow KEYSTONE13



```
remove TP follow kyloren 15 IO
      layout 空間不足
```


(Blanking)


<Core Design>

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Title			
(Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 33 of	106

Main Func = USB2.0

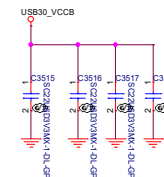
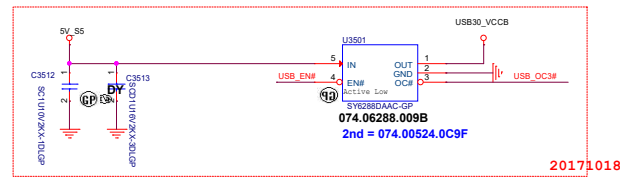
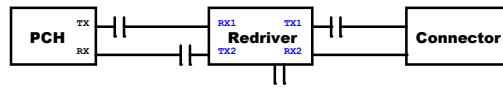
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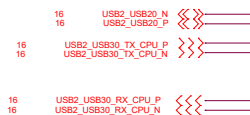
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Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 34 of	106

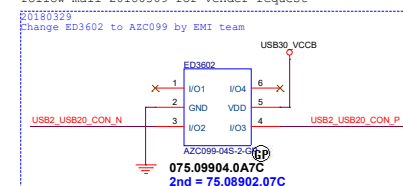
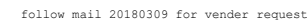
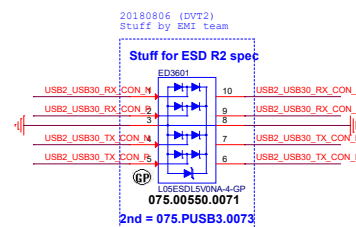
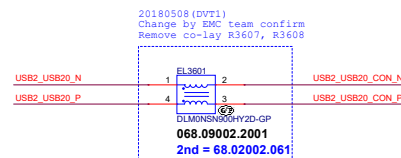
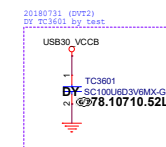
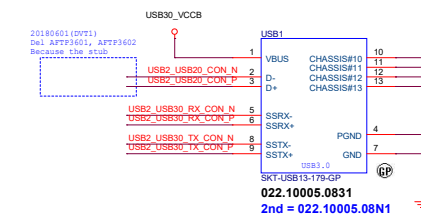
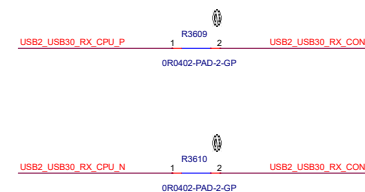
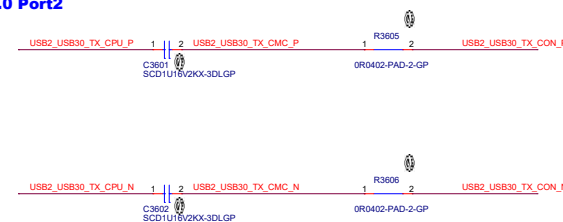
4
Main Func = USB3.0 Port2

```
usb3.0 follow RO 15
```





USB3.0 Port2




USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

Main Func = USB3.0 Port2


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<Core Design>

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Title (Reserved)					
Size	Document Number Pinehill-KBL-R				Rev A00
Date: Wednesday, September 26, 2018			Sheet	37	of 106

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Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 38	of 106

Main Func = Camera PMIC

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<Core Design>

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Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 39 of	106


Main Func = Power Plane & Sequence

follow bucky change to R2511



20170315 Remove_Anita

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sequence_(DS3/S0ix)(RSVD)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 41	of 106

Main Func = DIMM1
Main Func = DIMM2

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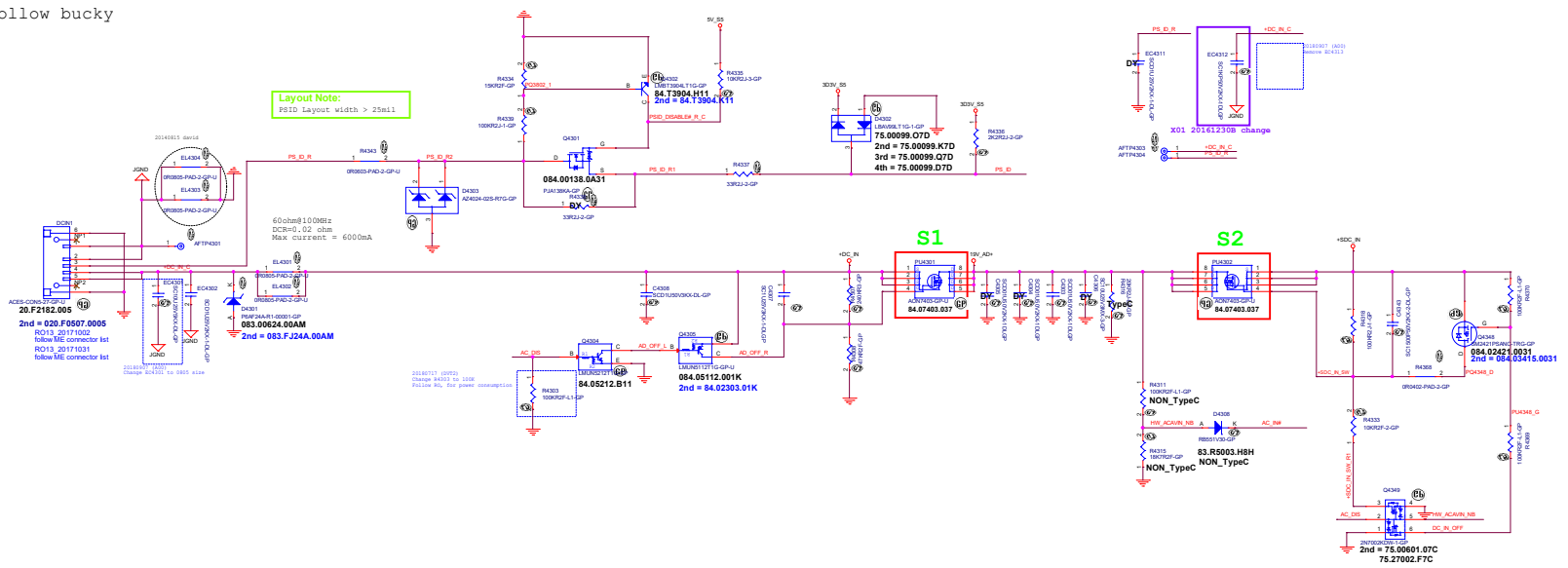
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title INT IO_(RSVD)		
Size A4	Document Number Pinehill-KBL-R	Rev A00
Date: Wednesday, September 26, 2018		Sheet 42 of 106

24	PS_ID	<<<
17,44	AC_RW	>>>
24	HW_ACORN_NB	<<<
24,44	PSAT_CHG_SMBCLK	<<>>
24,44	PSAT_CHG_SMBDAT	<<>>
24,44	PSAT_PRESH	<<>>
24	AC_DS	>>>

ollow bucky

Layout Note:
PSID Layout w/

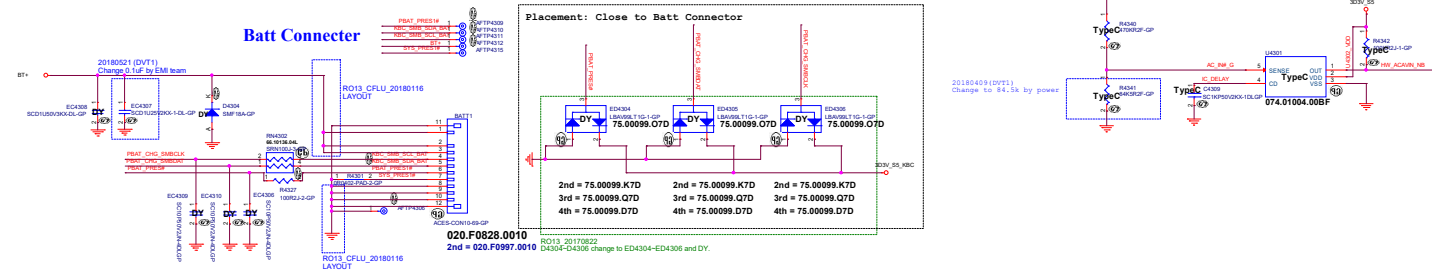


Main Func = M-BAT Input

Batt Connector

Placement: Close to Batt Connector

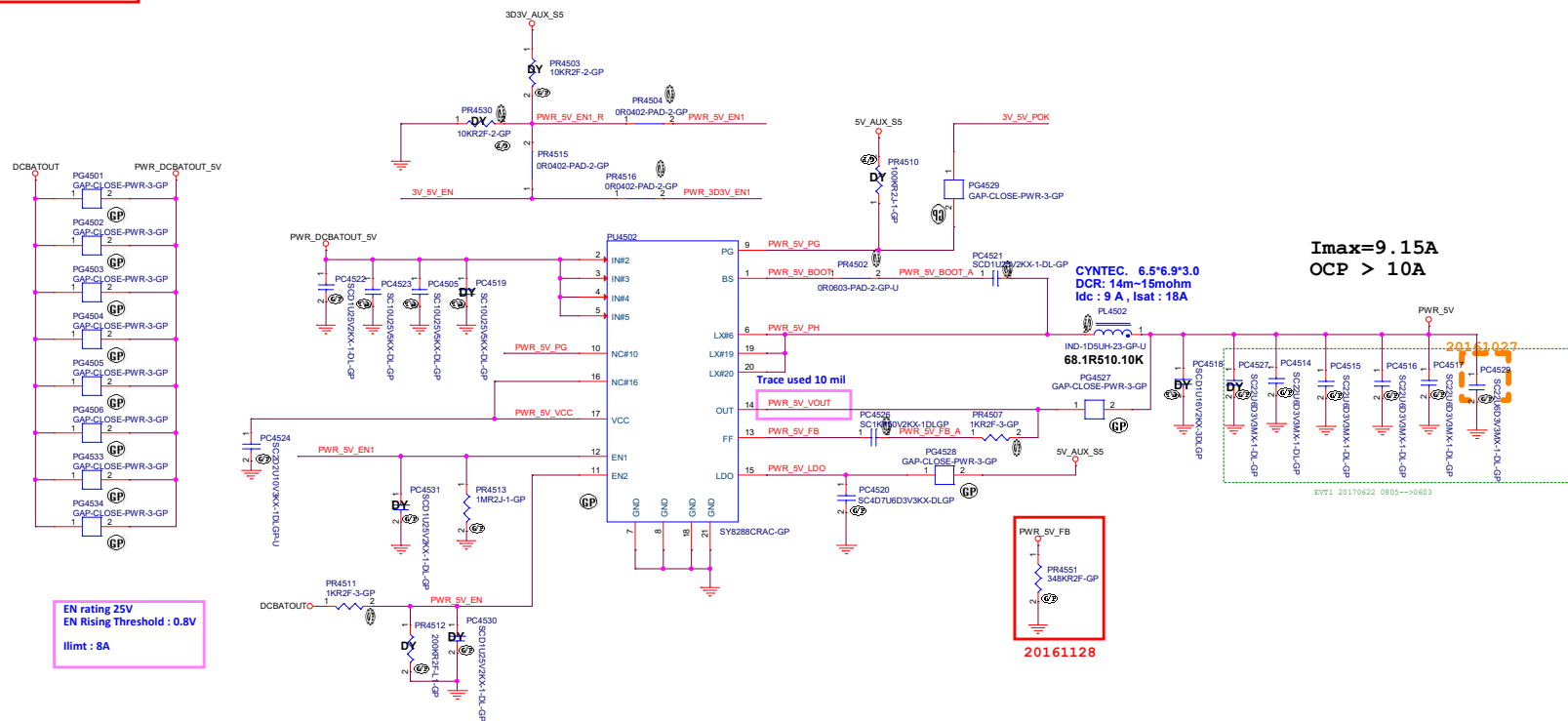
Barrel Adapter Plug-in Detect



<https://vinafix.com>

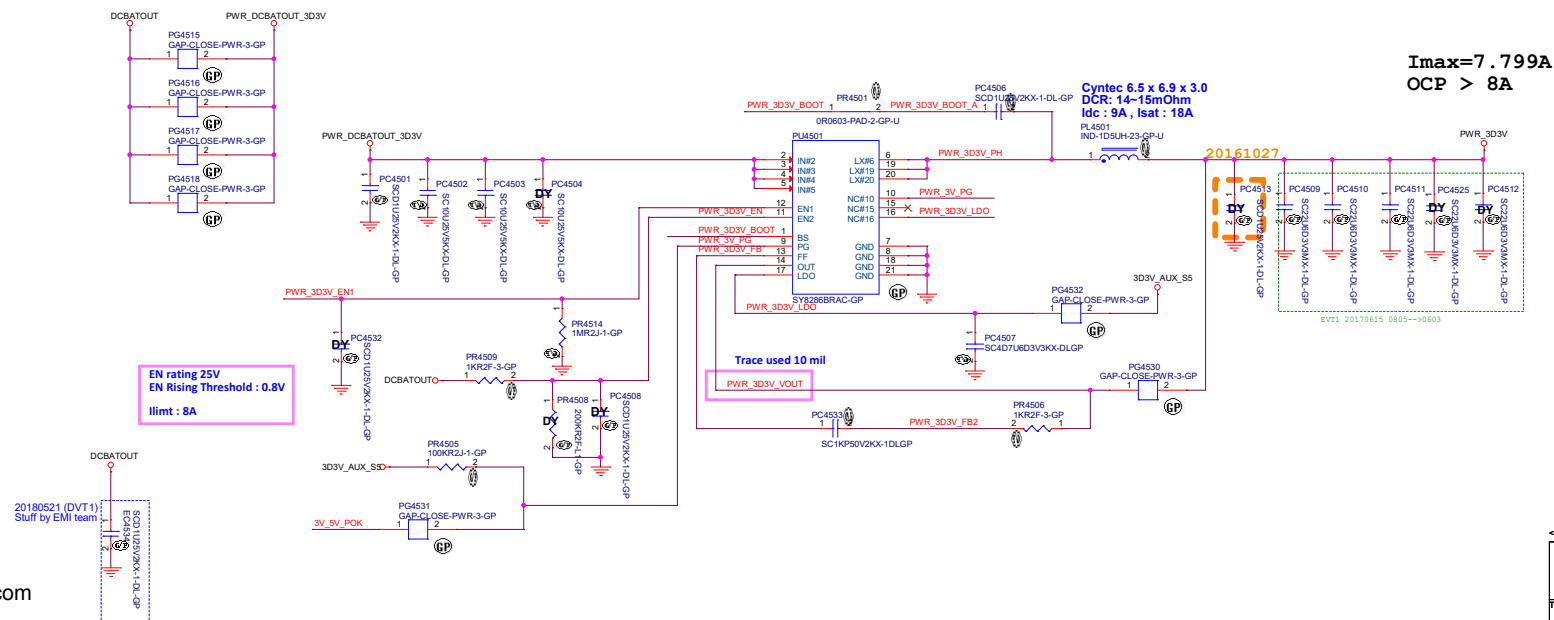
SSID = PWR.Plane.Regulator_5V

40 3V_5V_EN >>>
25,40,45 3V_5V_POK <<<



SSID = PWR.Plane.Regulator_3D3V

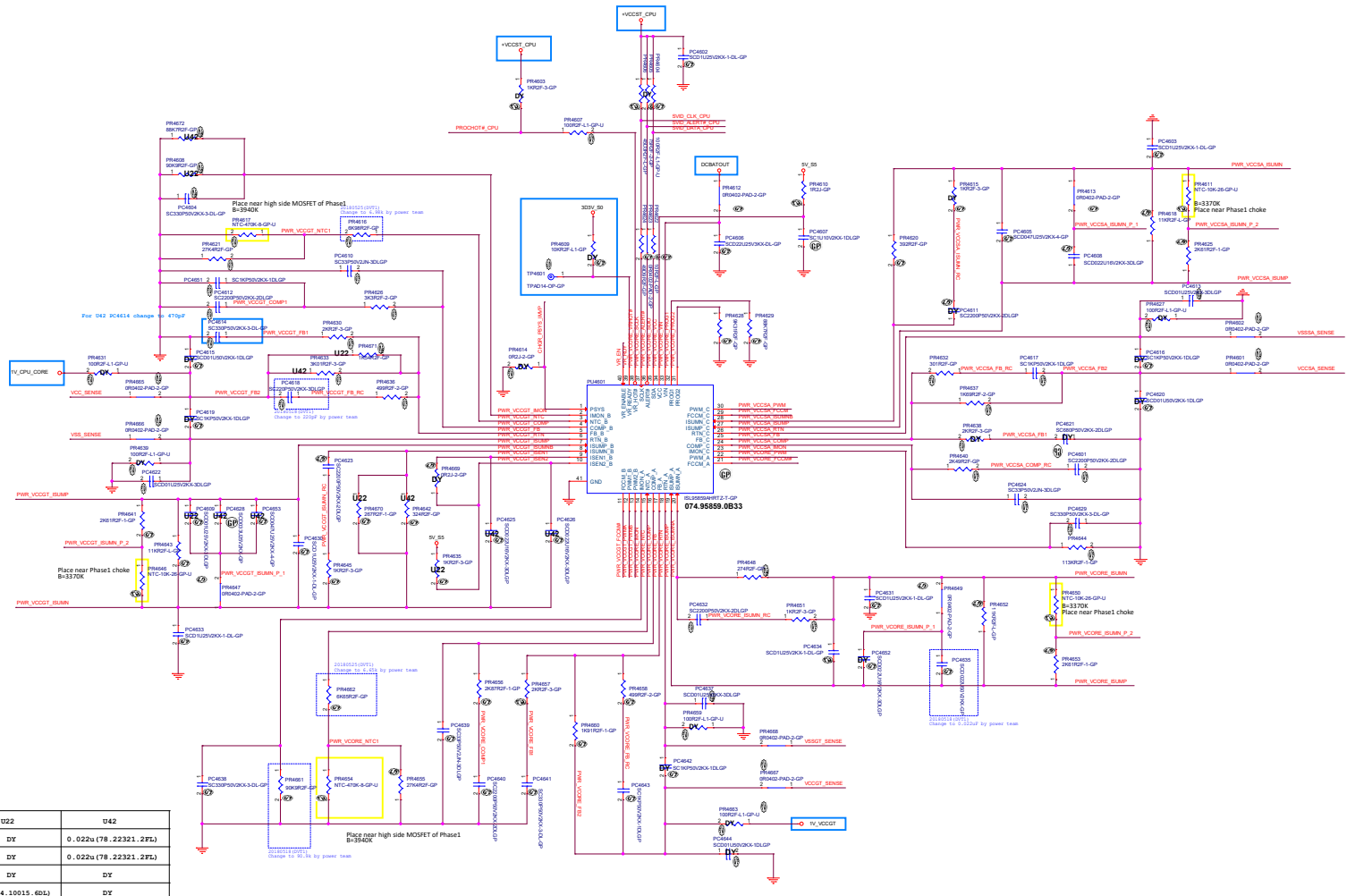
25,40,45 3V_5V_POK <<<



<https://www.afix.com>

<Core Design>

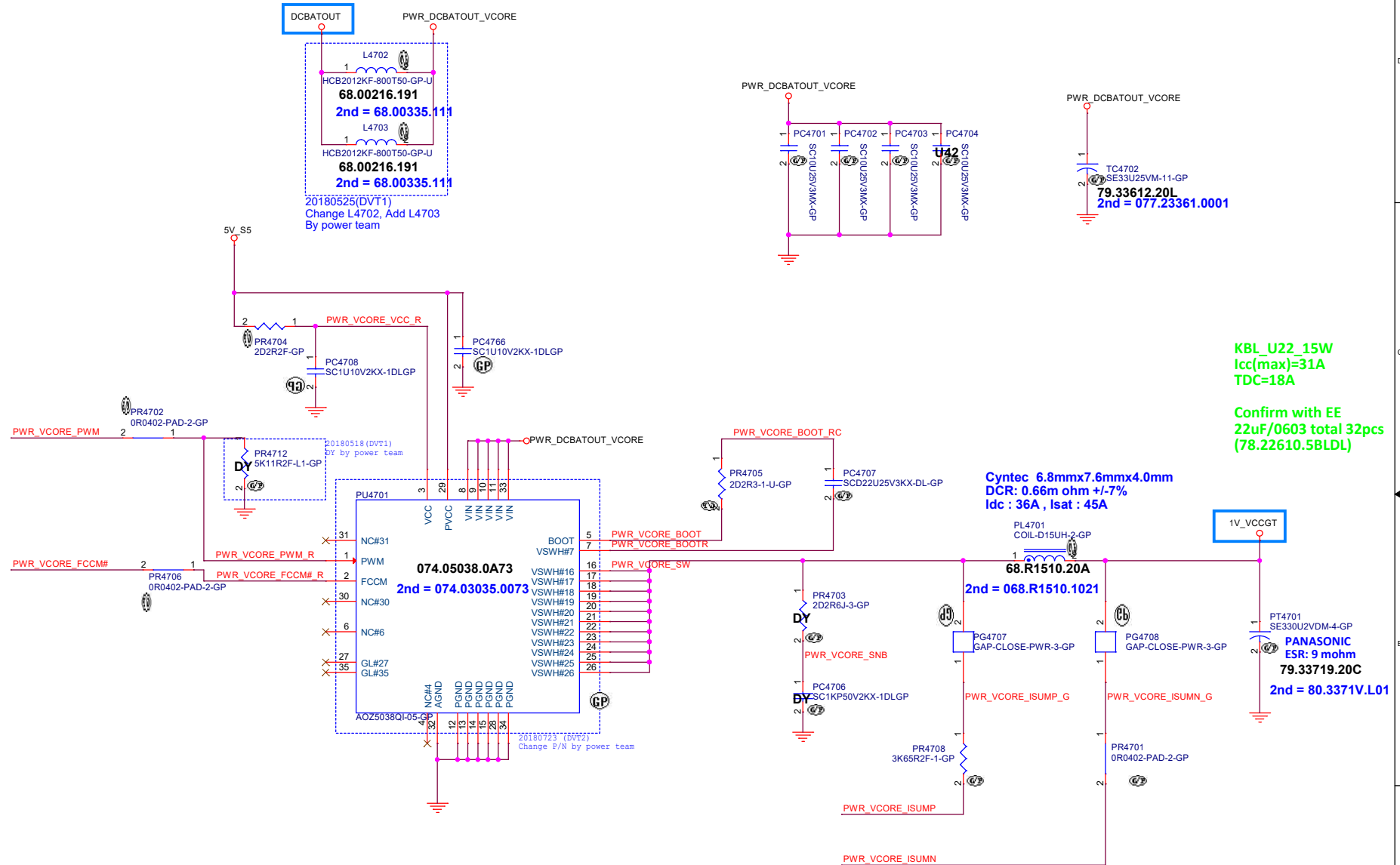
- 7 SVD_CLK_CPU <<<
- 7 SVD_ALERT1_CPU <<<
- 7 SVD_DATA_CPU <<<
- 7 VCC_SENSE <<<
- 7 VSS_SENSE <<<
- 48 PWR_VCCST_BUM >>>
- 48 PWR_VCCST_BUM >>>
- 48 PWR_VCCST_BUM >>>
- 48 PWR_VCCST_BUM >>>
- 7 VCCST_SENSE <<<
- 7 VCCST_SENSE <<<
- 47 PWR_VCORE_BUM >>>
- 47 PWR_VCORE_BUM >>>
- 50 PWR_VCCA_BUM >>>
- 50 PWR_VCCA_BUM >>>
- 7 VCCA_SENSE <<<
- 7 VCCA_SENSE <<<
- 48 PWR_VCCST_FCOM >>>
- 48 PWR_VCCST_FCOM >>>
- 48 PWR_VCCST_FCOM >>>
- 48 PWR_VCCST_FCOM >>>
- 50 PWR_VCCA_PWM >>>
- 50 PWR_VCCA_PWM >>>
- 47 PWR_VCORE_PWM >>>
- 47 PWR_VCORE_PWM >>>
- 40 VLEW >>>
- 5,24,44 PROCHOT6_CPU <<<
- 44 CHGR_PVSV_MMP >>>



	U22	U42
PC4625	DY	0.022u(78.22321,2PL)
PC4626	DY	0.022u(78.22321,2PL)
PC4669	DY	DY
PM4635	1K(64.30015,6DL)	DY
PM4642	267(64.26705,6DL)	316(64.31605,6DL)
PC4630	0.1u(78.10422,5PL)	0.1u(78.10422,5PL)
PC4628	0.01u(78.10334,10L)	0.022u(78.22322,2PL)
PC4653	DY	47n(78.47322,2PL)
PM4633	1.54K(64.15415,6DL)	3.01K(64.30115,6DL)
PM4608	88.7K(64.88725,6DL)	88.7K(64.88725,6DL)

Main Func = CPU CORE

PWR_VCORE_PWM >>>
PWR_VCORE_FCCM# >>>
PWR_VCORE_ISUMP <<<
PWR_VCORE_ISUMN <<<



<Core Design>

DELL		Wistron Corporation	
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Title: ISL95859C_CPU_VCORE(2/3)			
Size: A3	Document Number: Pinehills	Rev: A00	
Date: Wednesday, September 26, 2018	Sheet: 47	of: 105	

<https://vinafix.com>

<Core Design>

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Size	Document Number				Rev
A2	Bucky WSL				A00
Date: Wednesday, September 26, 2018 Sheet 49 of 105					

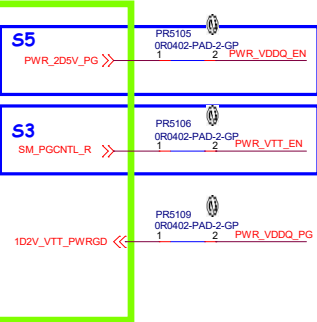
```

46      PWR_VCCSA_PWM >>> _____
46      PWR_VCCSA_ISUMP <<< _____
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      PWR_VCCSA_FCCM >>> _____

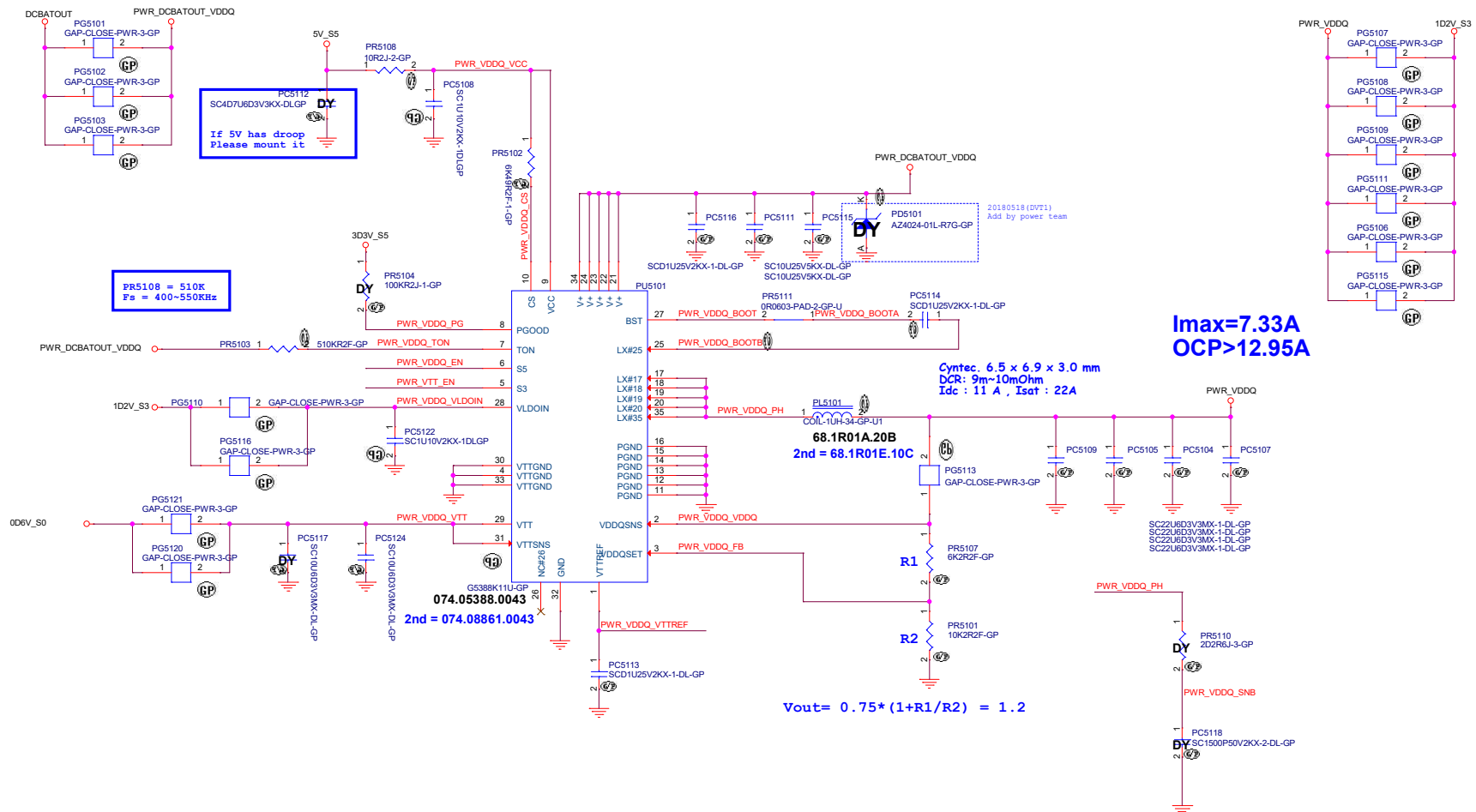
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OFFPAGE



Need EE check



<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File: **VDDQ/VTT**

Size: Custom, Document Number: **Pinehills**, Rev: **A00**

Date: Monday, October 01, 2018, Sheet: 51 of 105

40 1D0V_S5_PWRGD <<< _____

25,54 3V_5V_DSW_OK >>> _____



Design Current : 6.839A
OCP = 11A

SSID = PWR.Plane.Regulator_VCCIO/VCCPRIM_CORE

<https://vinafix.com>

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

File

(Reserved)

Size
A2

Document Number
Kyloren 15" KBL-U

Rev
A00

Date: Wednesday, September 26, 2018

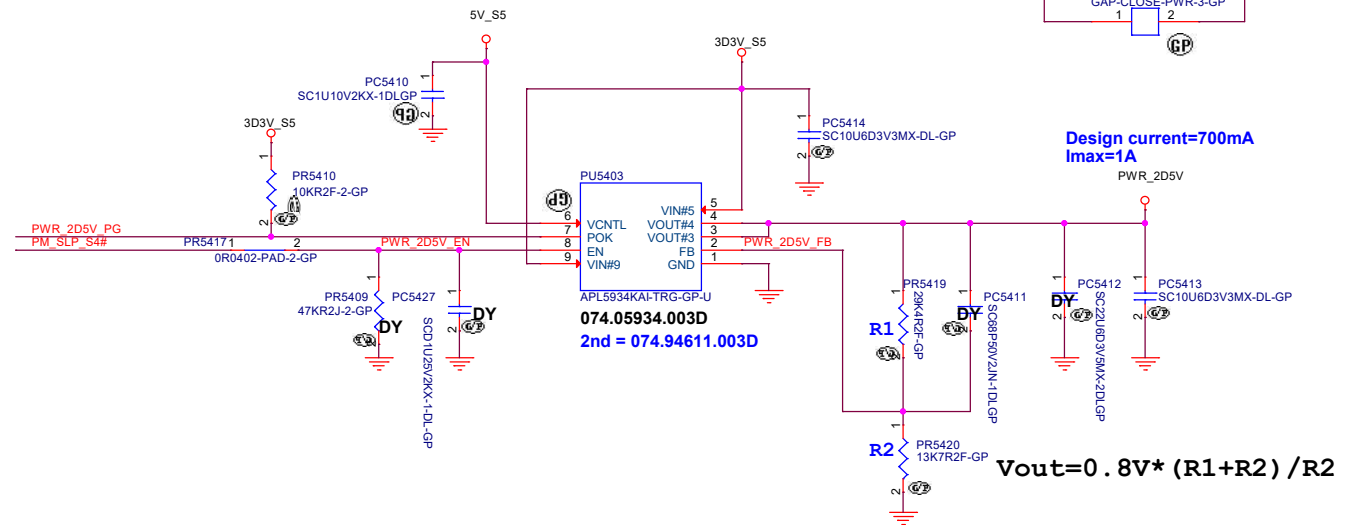
Sheet 53 of 106

Main Func = 2D5V/ 1D8V

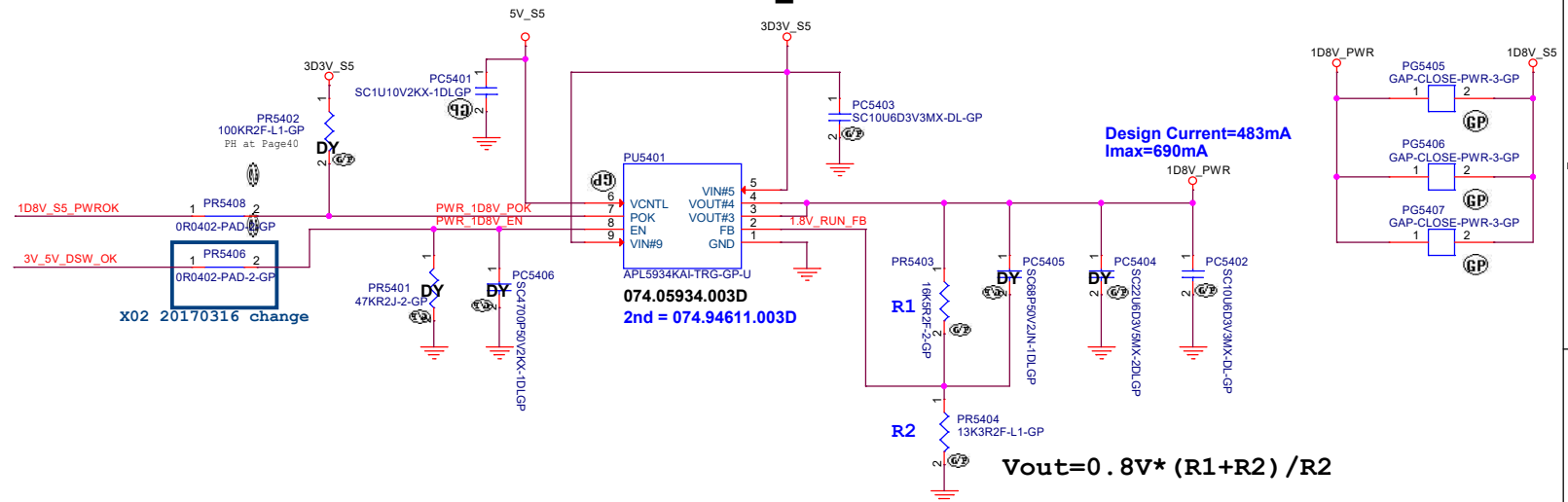
Main Func = 2D5V/ 1D8V

17,40 PM_SLP_S4# >>>
51 PWR_2D5V_PG <<<
25,52 3V_5V_DSW_OK >>>
24,40 1D8V_S5_PWROK <<<

APL5934 for 2D5V

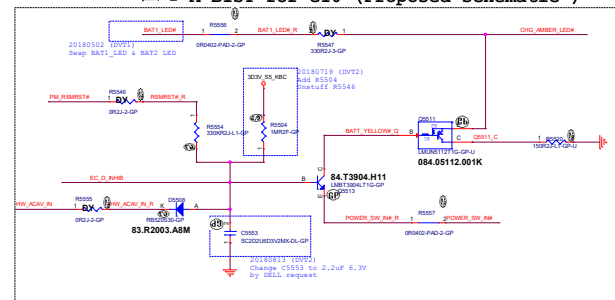
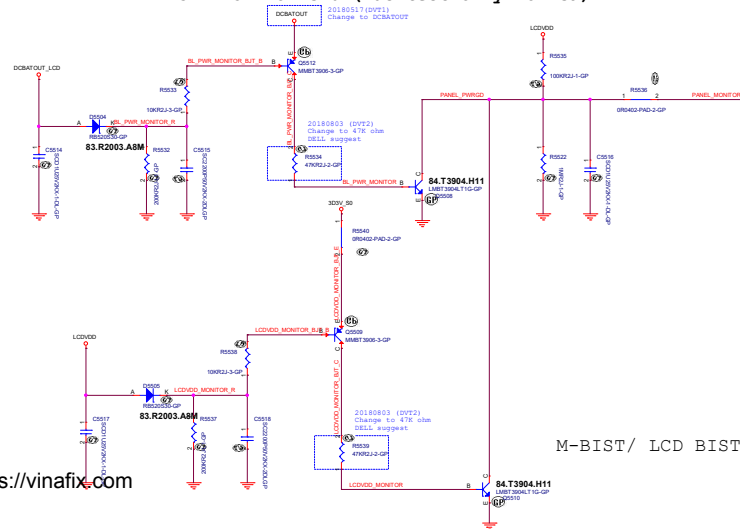
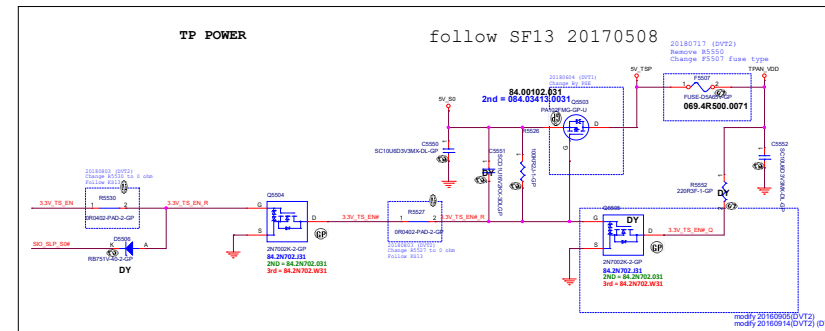
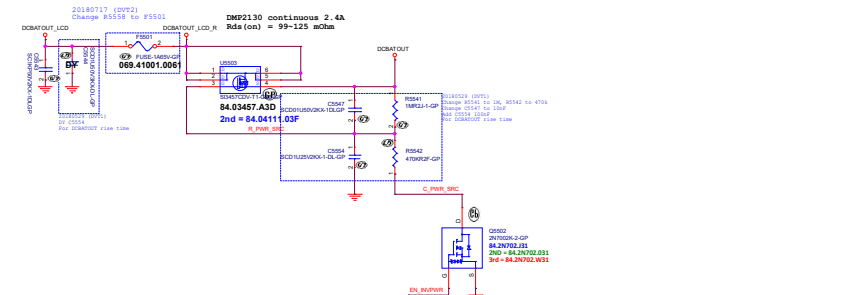
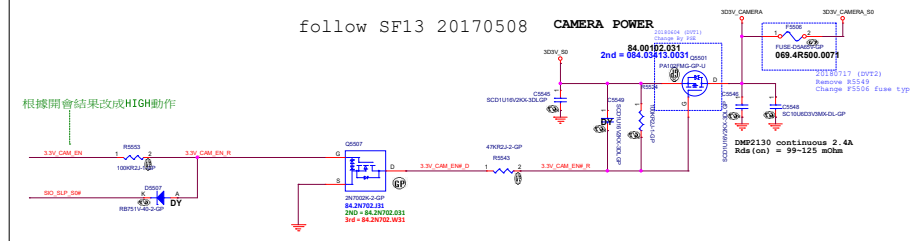
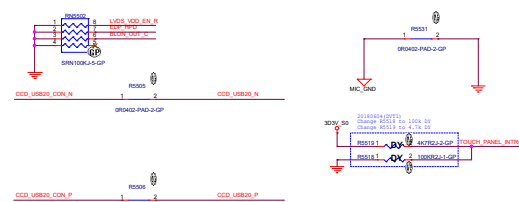
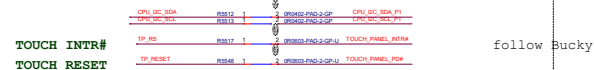
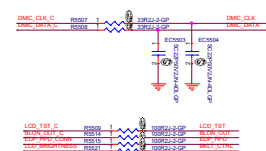
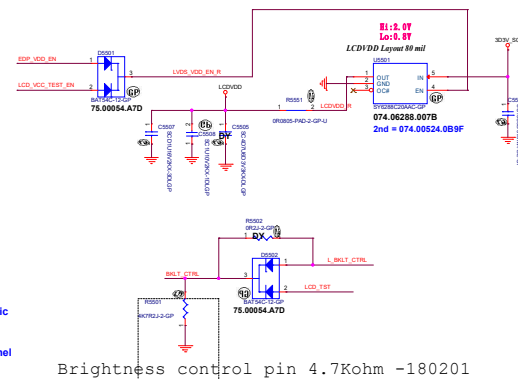
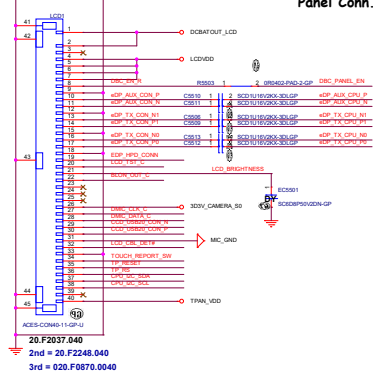


APL5934 for 1D8V_S5



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Type: (Reserved)			
Size: A3	Document Number: Kyloren 15" KBL-U		Rev: A00
Date: Wednesday, September 26, 2018	Sheet: 54	of 106	




M-BIST/ LCD BIST -1890201

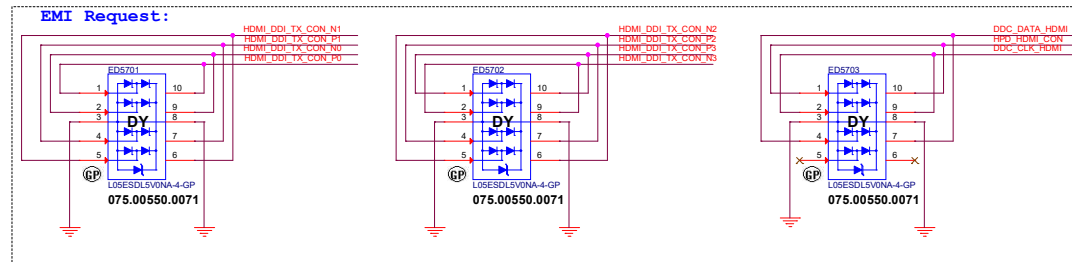
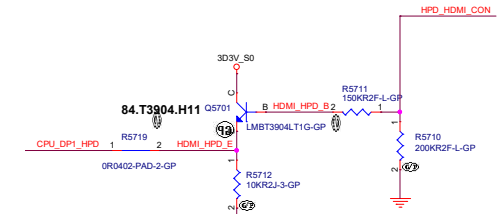
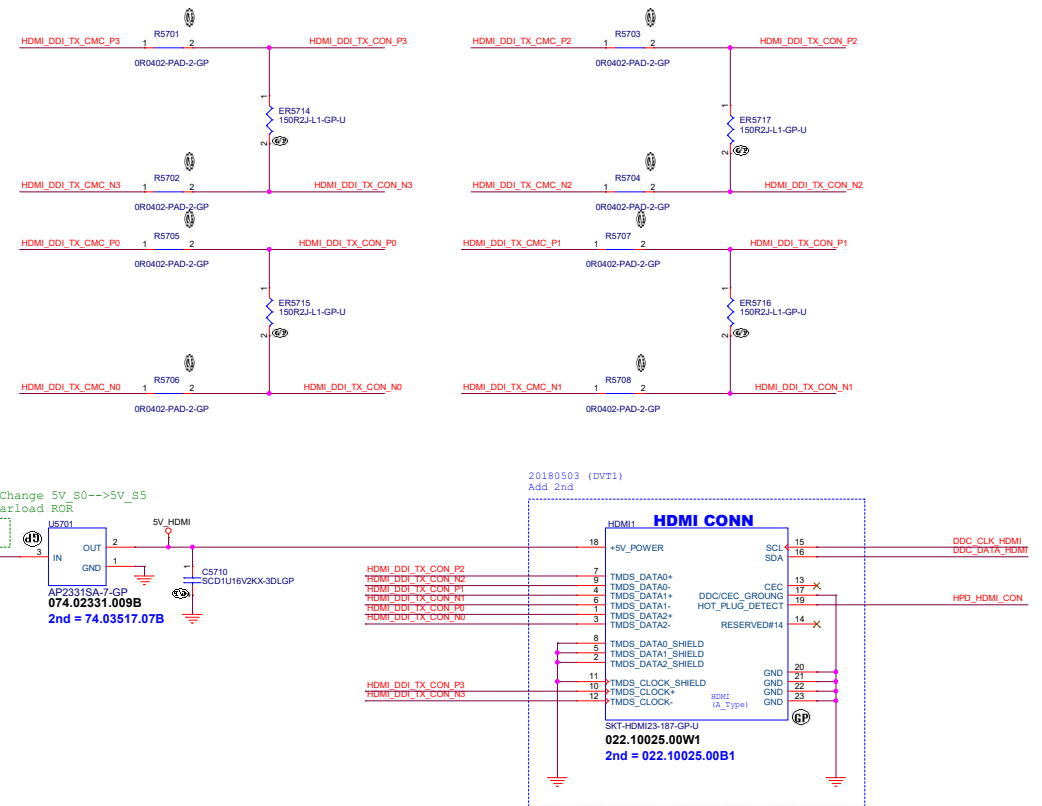
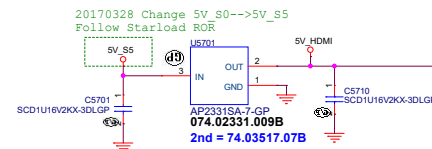
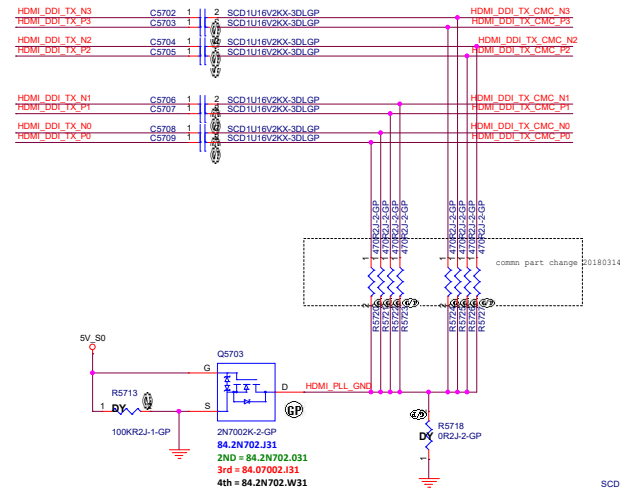
Main Func = CRT

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Title (Reserved)		
Size A4	Document Number Pinehill-KBL-R	Rev A00
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follow keystone 13



Main Func = DP

(Blanking)


<Core Design>

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Title (Reserved)		
Size A4	Document Number Pinehill-KBL-R	Rev A00
Date: Wednesday, September 26, 2018		Sheet 58 of 106

Main Func = DVI

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 59 of	106

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Title (Blanking)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 60	of 106

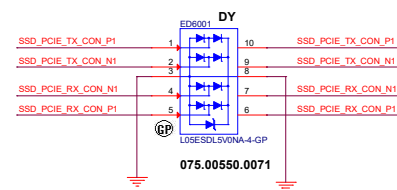
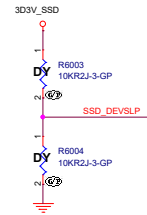
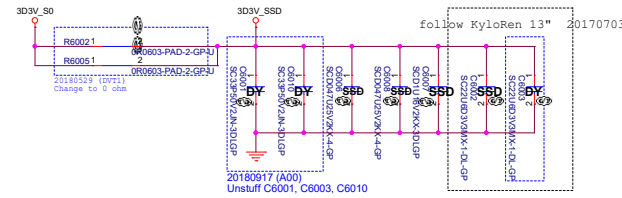
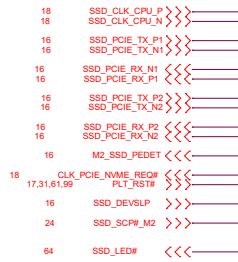
SSID = WIRELESS *NGFF(WWAN/SSD)*

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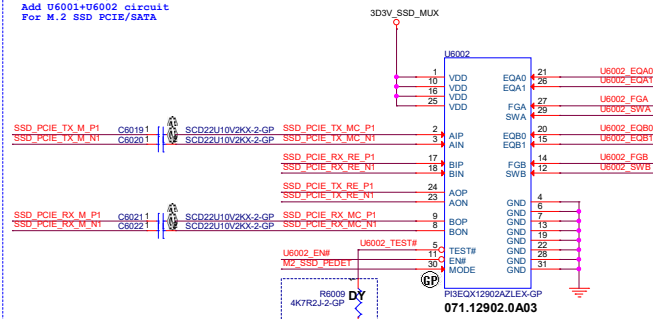
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Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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follow KyloRen 15



MUX+Re-driver

```
20180601(DVT1)
Add U6001+U6002 circuit
For M.2 SSD PCIE/SATA
```



20180716(DVT2)
DY R6009 for slumber mode

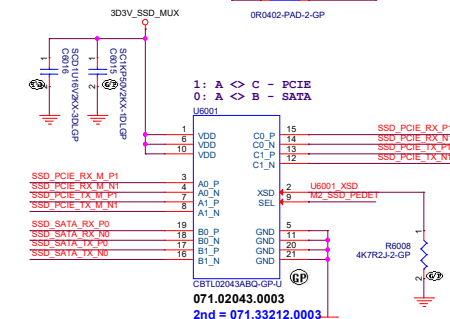
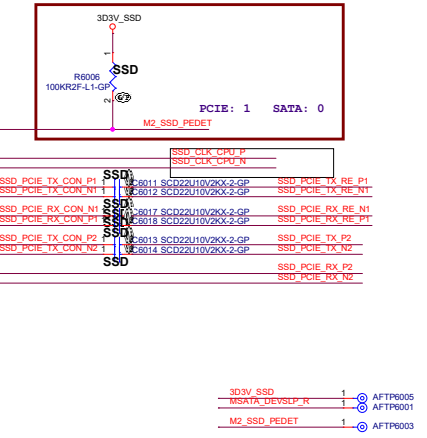
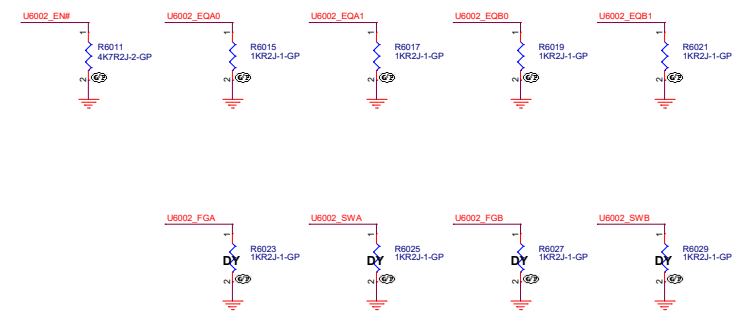


Table 13-12.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen2 3/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the [Chapter 3, "General Differential Signals Design Guidelines"](#) along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: To ensure lane that needs to support either PCIe* Gen2 devices or PCIe* Gen3 devices, follow the PCIe* Gen3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**



<Core Design>



Title	INT IO (NGFF-SSD M.2)
-------	------------------------------

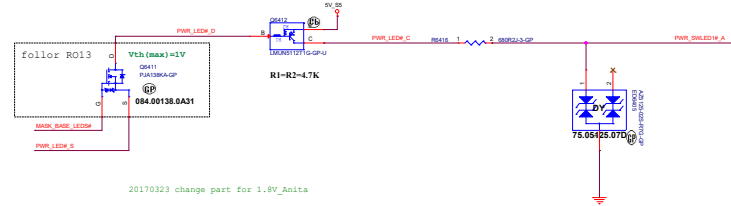
Size A2	Document Number DRAX13 KBL	Rev A00
Date: Wednesday, September 26, 2018	Sheet of 63	of 106

Main Func = Power BTN

Power LED LOW activated from KBC GPIO

follow keystone 13

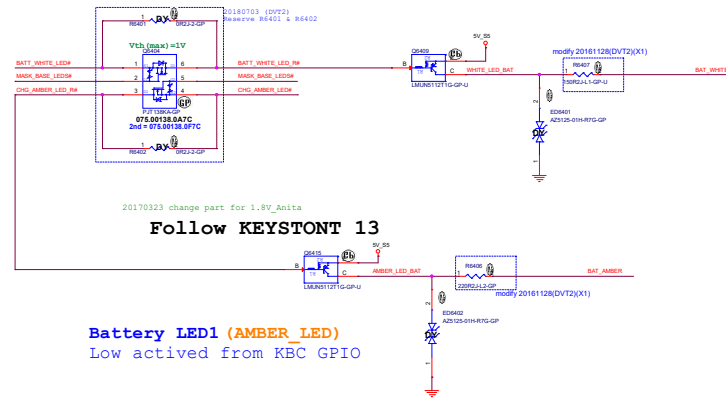
POWER BUTTON LED



Main Func = Battery LED

follow keystone 13

Battery LED2 (WHITE_LED) Low activated from KBC GPIO

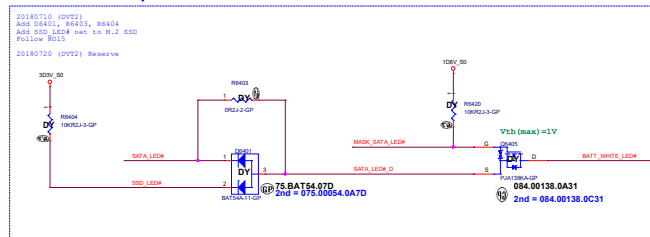


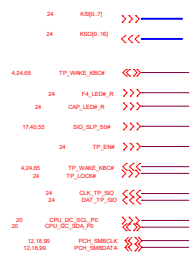
Follow KEYSTONT 13

Battery LED1 (AMBER_LED) Low activated from KBC GPIO

Main Func = SATA/PCIE SSD LED

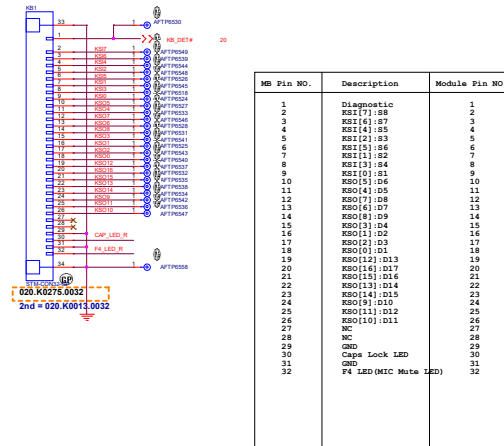
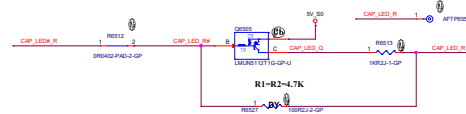
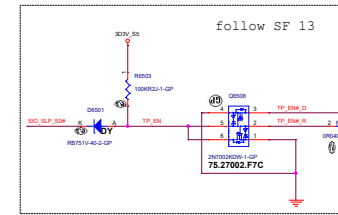
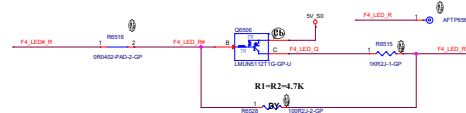
SATA/PCIE SSD LED



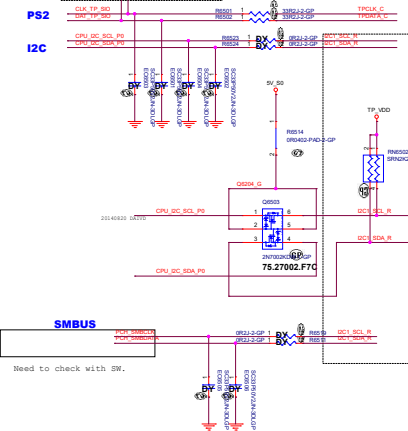


follow SF 13

Internal KeyBoard Connector

CAP LED Control
LOW acted from KBC GPIOFA4 LED (MIC Mute LED) Control
LOW acted from KBC GPIO

Support PTP

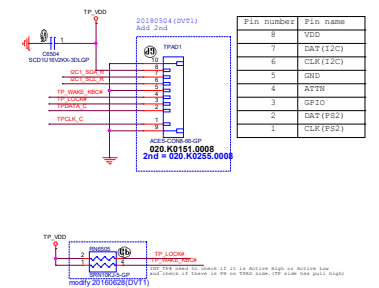


SMBUS

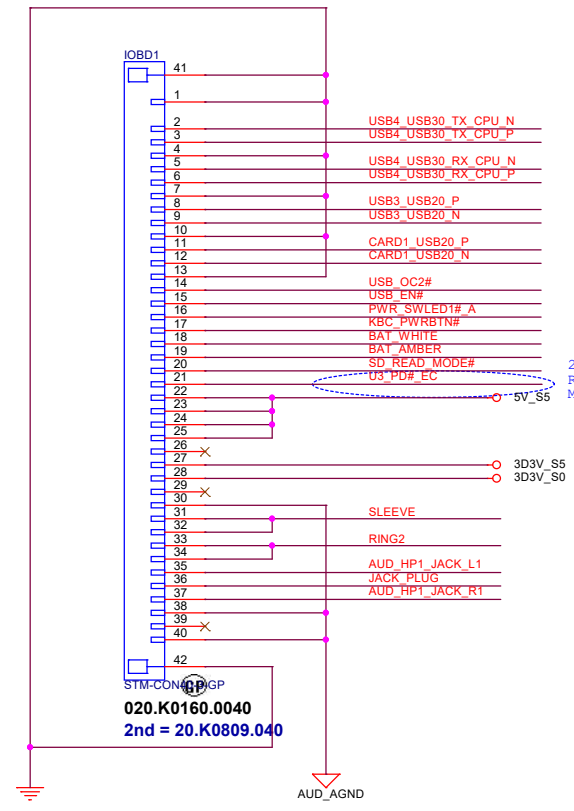
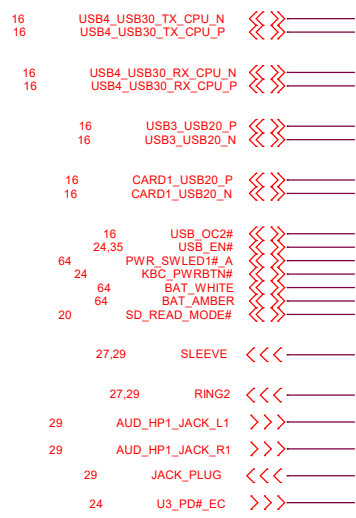
Need to check with SW.

follow SF 13

Precision Touch Pad Connector



Main Func = IO Connector



USB Part3 USB3.0

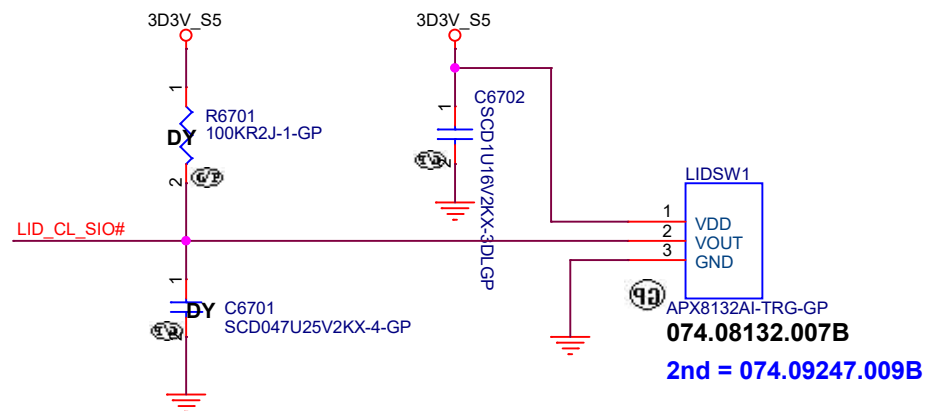
USB Part3 USB2.0

Card Reader

20180703 (DVT2)
Reserve U3 PD# pin
Modify IOBD pin define

Main Func = Hall Sensor

24,64 LID_CL_SIO# <<—



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

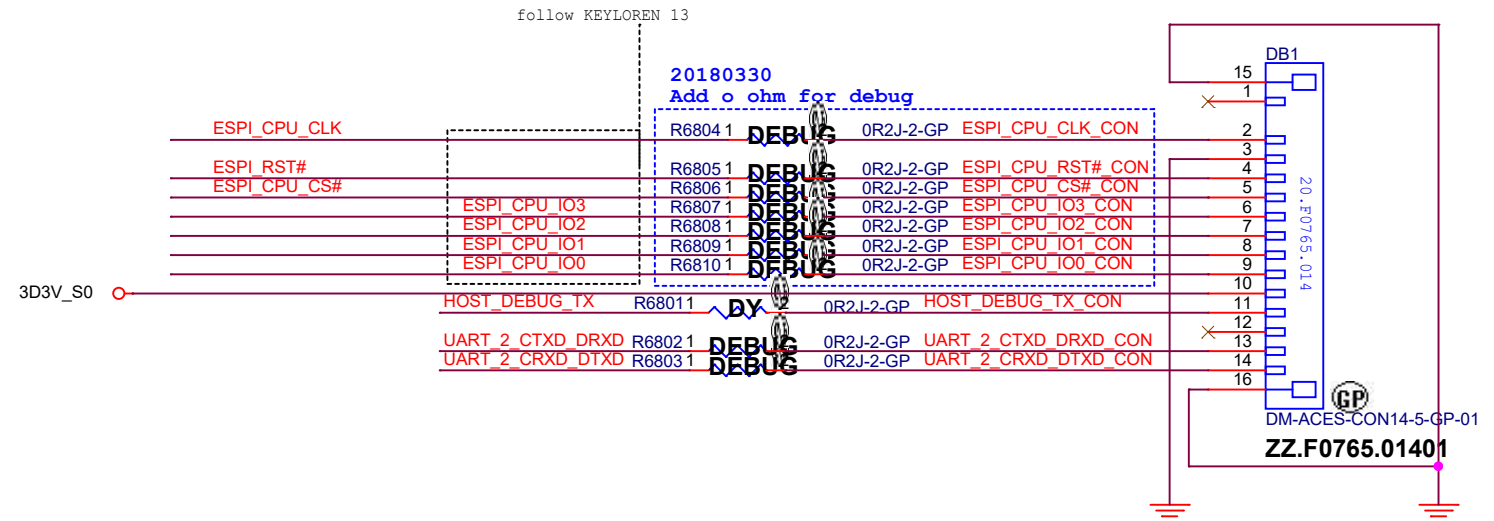
<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPIO Expander (IT8010FN)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = Debug

follow Bucky

Debug Connector



<Core Design>



Wistron Corporation

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Title

Dubug connector

Size
A4

Document Number

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of

106

Main Func = SENSOR HUB

(Blanking)

<Core Design>

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Title			
Reserved			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = TBD

(Blanking)

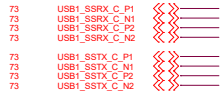
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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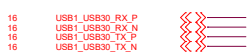
DisplayPort Source



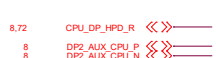
USB3.0 TYPEC CONNECTOR



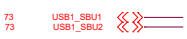
USB HOST



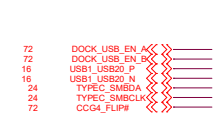
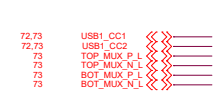
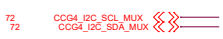
DisplayPort HPD



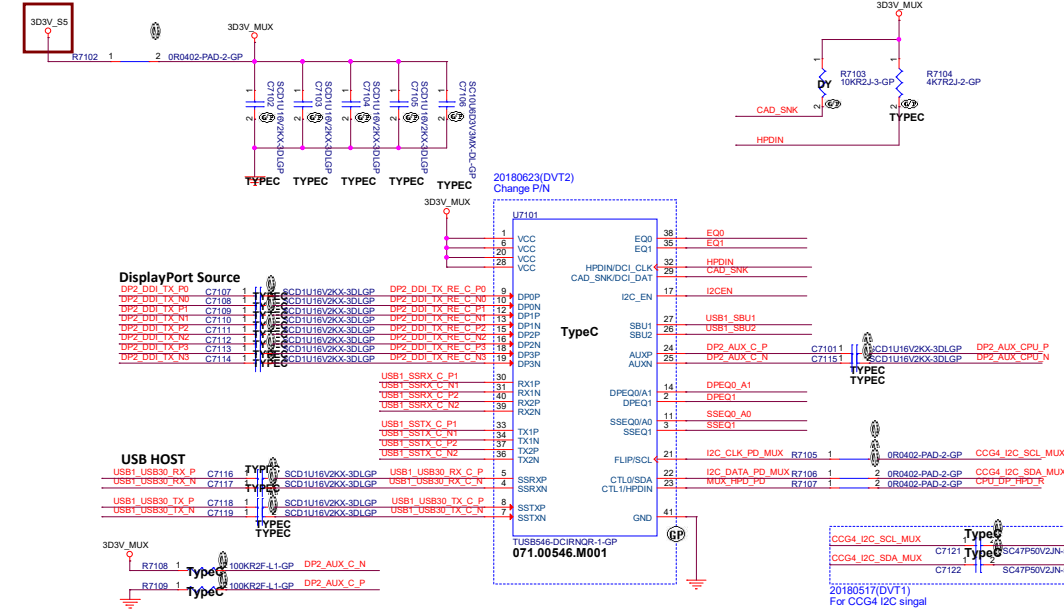
TypeC CC



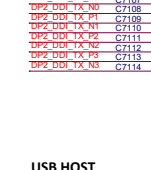
MUX I2C



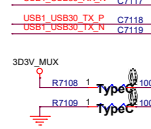
For displayport function at dead battery condition



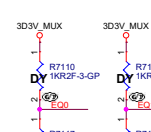
DisplayPort Source



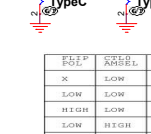
USB HOST



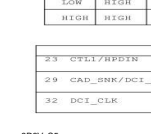
USB HOST



USB HOST



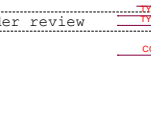
USB HOST



USB HOST



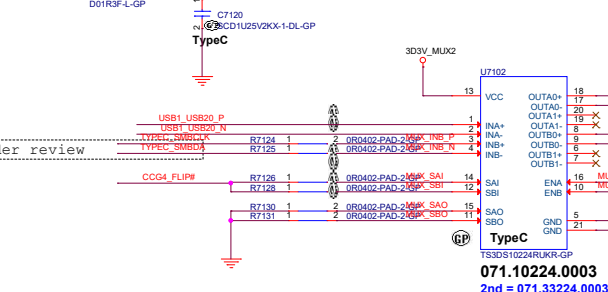
USB HOST



USB HOST



I2C/USB2.0 MUX



ENA, ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	Hi-Z	Hi-Z	Hi-Z	Hi-Z
01	Hi-Z	Hi-Z	-	-
10	-	-	Hi-Z	Hi-Z
11	-	-	-	-

https://vinafix.com

FOLLOW BUCKY

FOLLOW SF

SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	-	INA	-
1010	INA	-	INB	-

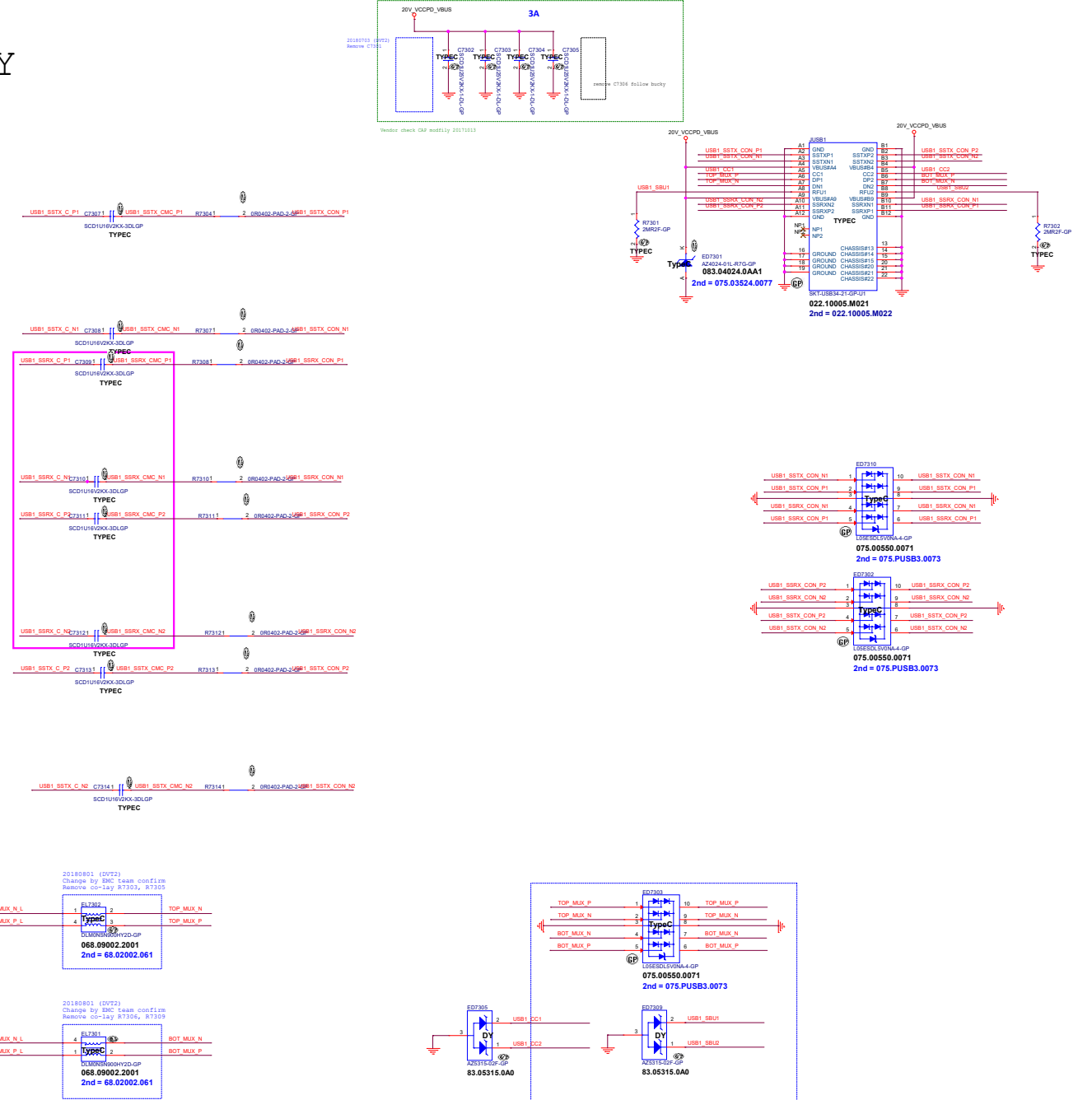
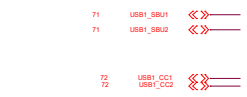
<Core Design>

FOLLOW BUCKY

USB3.0 TYPEC CONNECTOR



TypeC CC



Follow Bucky
P/N: 071.17030.000U
C TYPE-C PD CTRL SN1703018ZQZR BGA 96P

GPIO0 (USB_OC0#): default HI Set open drain to meet unplug , GPIO is high condition
GPIO1 (PD_OVP_TRIP_P1): default LO OK
GPIO4 (DP1 HPD CPU): default LO OK
GPIO6 (PD_VBUS_C_CTRL1): default LO OK
GPIO7 (VBUS_P_CTRL): default LO OK

By Dell mail 2018/01/30 10:00

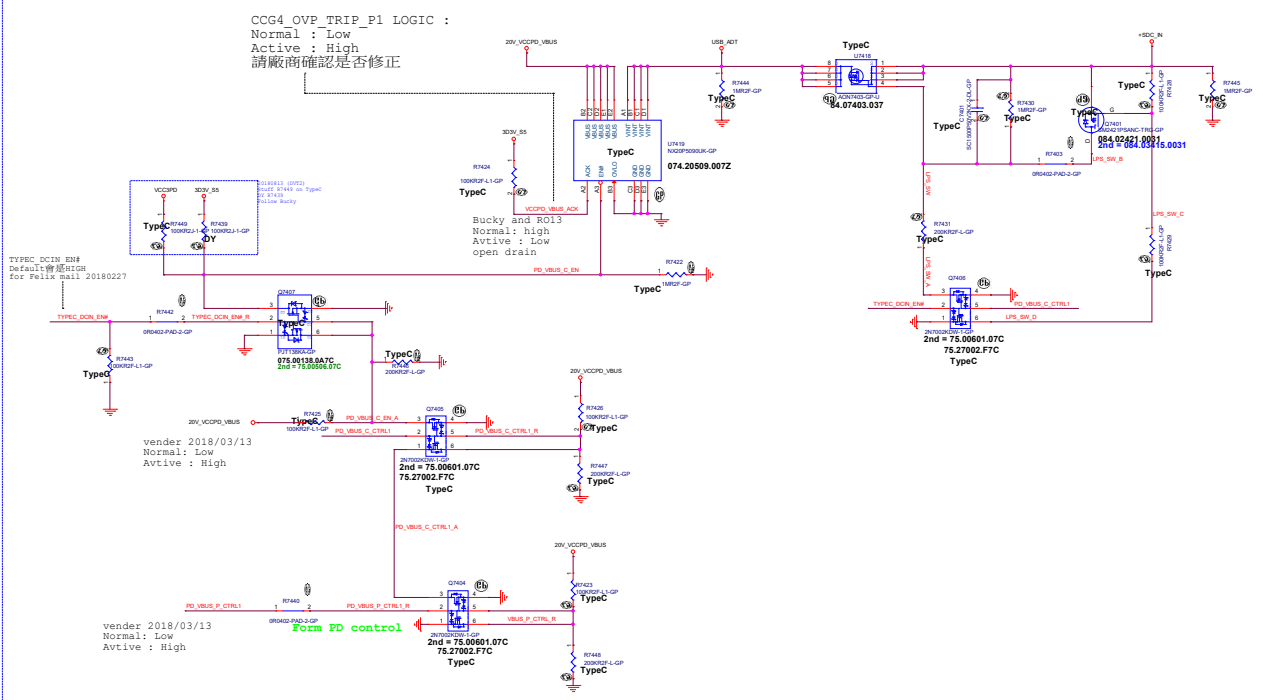
vender 2018/03/13
Normal: Low
Active: High

vender 2018/03/13
Normal: Low
Active: High

Follow GGC4 vender review 20180301- Jeff

20180427 (DVT1)
Follow RO13 design

CCG4_OVP_TRIP_P1 LOGIC :
Normal : Low
Active : High
請廠商確認是否修正



vender 2018/03/13
Normal: Low
Active: High

vender 2018/03/13
Normal: Low
Active: High

FOLLOW RO13

<https://vinafix.com>

+3D3V_VDD_DCIN

DC_IN_OK invert

Barrel Adapter Plug-in Detect

Barrel Adapter Plug-in Disable S4

PD_VBUS_C_CTRL1 invert

Main Func = Thunderbolt

(Blanking)

<Core Design>



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Title

(Reserved)

Size
A4

Document Number


Pinehill-KBL-R

Rev
A00

Main Func = dGPU

(Blanking)


<Core Design>

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Title (Reserved)			
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Main Func = dGPU

(Blanking)


<Core Design>

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Title (Reserved)			
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Main Func = dGPU

(Blanking)


<Core Design>

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Title (Reserved)			
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Main Func = dGPU

(Blanking)


<Core Design>

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Title (Reserved)			
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Main Func = dGPU

(Blanking)


<Core Design>

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Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = dGPU

(Blanking)


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = dGPU

(Blanking)


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 82 of	106

Main Func = dGPU

(Blanking)


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 83 of	106

Main Func = dGPU

(Blanking)


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = dGFX_CORE

(Blanking)


<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
Size A4		Document Number Pinehill-KBL-R			Rev A00
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Main Func = dGPU

(Blanking)

<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = SWITCHABLE GFX LCD

(Blanking)

<https://vinafix.com>


<Core Design>

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Title			
(Reserved)			
Size A3	Document Number Pinehill-KBL-R		Rev A00
Date: Wednesday, September 26, 2018		Sheet 87 of	106

Main Func = Reserved

(Blanking)


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = NFC

(Blanking)


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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SSID = TPM

(Blanking)

<Core Design>



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Title

(Reserved)

Size
A3

Document Number
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A00

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(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)		
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5

4

3

2

1

D

D

C

C

B

B

A

A

(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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(Blanking)

<Core Design>

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Title			
(Reserved)			
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<Core Design>

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Title (Reserved)		
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5

4

3

2

1

D

D

C

C

B

B

A

A

(Blanking)

<Core Design>



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Title

(Reserved)

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Main Func = LAN

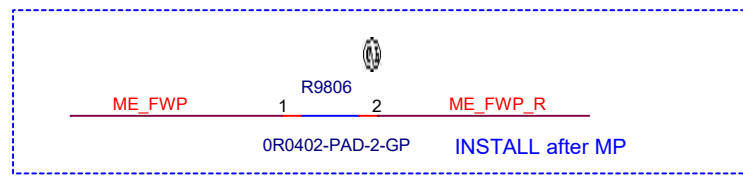
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Commercial (Intel LAN)			
Size A4	Document Number Pinehill-KBL-R		Rev A00
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Main Func = Firmware SW

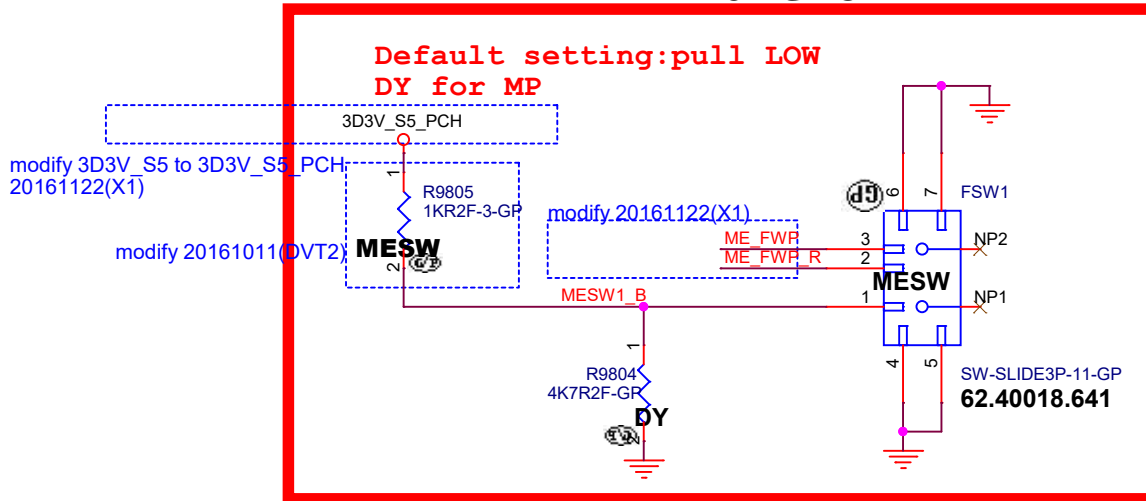
ME_FWP >>>
ME_FWP_R <<<



add 0 ohm
20161122(X1)

*Symbol same as
62.40018.461.

Firmware SW



modify 3D3V_S5 to 3D3V_S5_PCH
20161122(X1)

modify 20161011(DVT2)

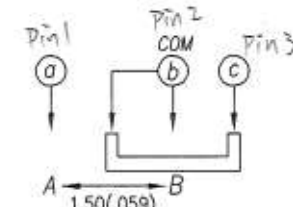
modify 20161122(X1)

modify 20161122(X1)

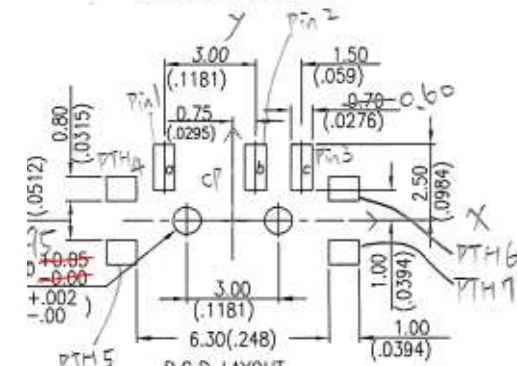
FSW1 change from 62.40018.691 to 62.40018.641
20160623(DVT1)

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

modify 20161122(X1)



CIRCUIT DIAGRAM



P.C.B LAYOUT

Top view

<Core Design>

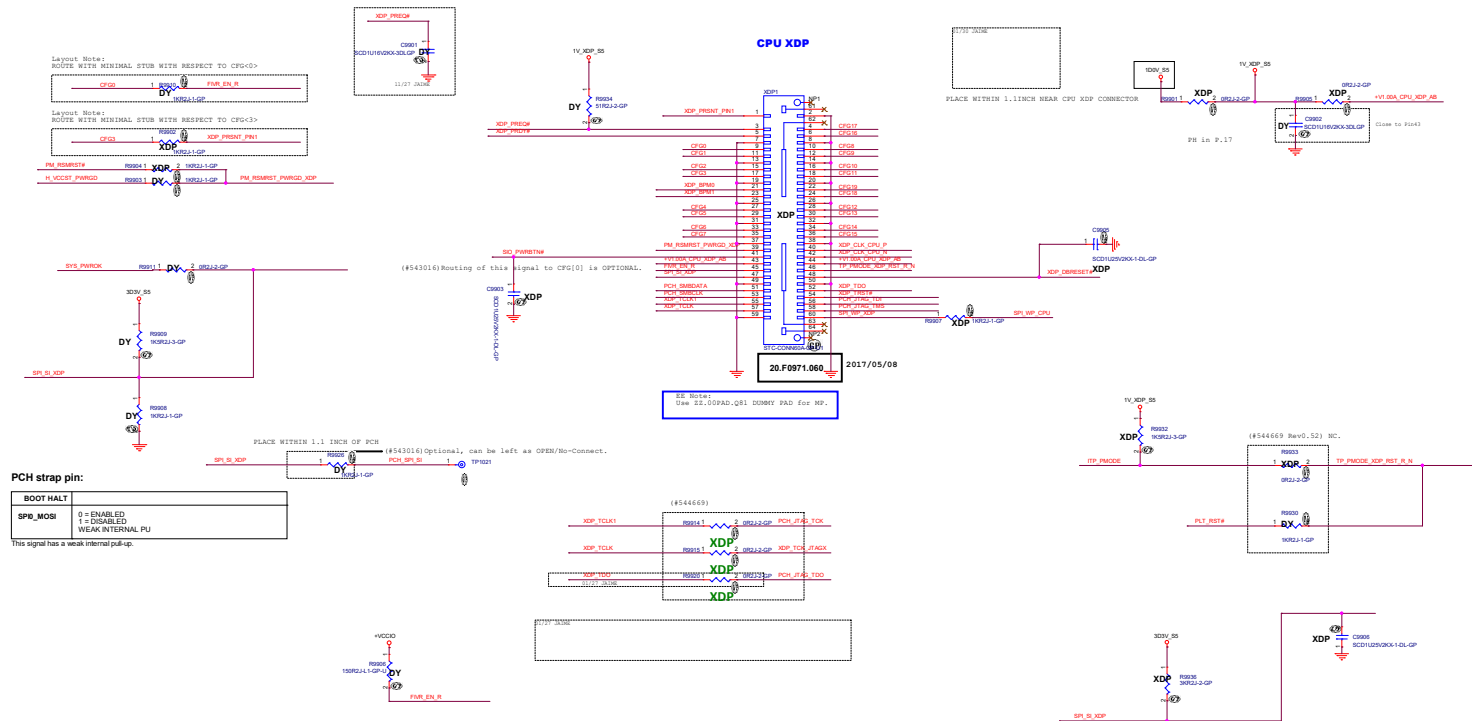


Wistron Corporation

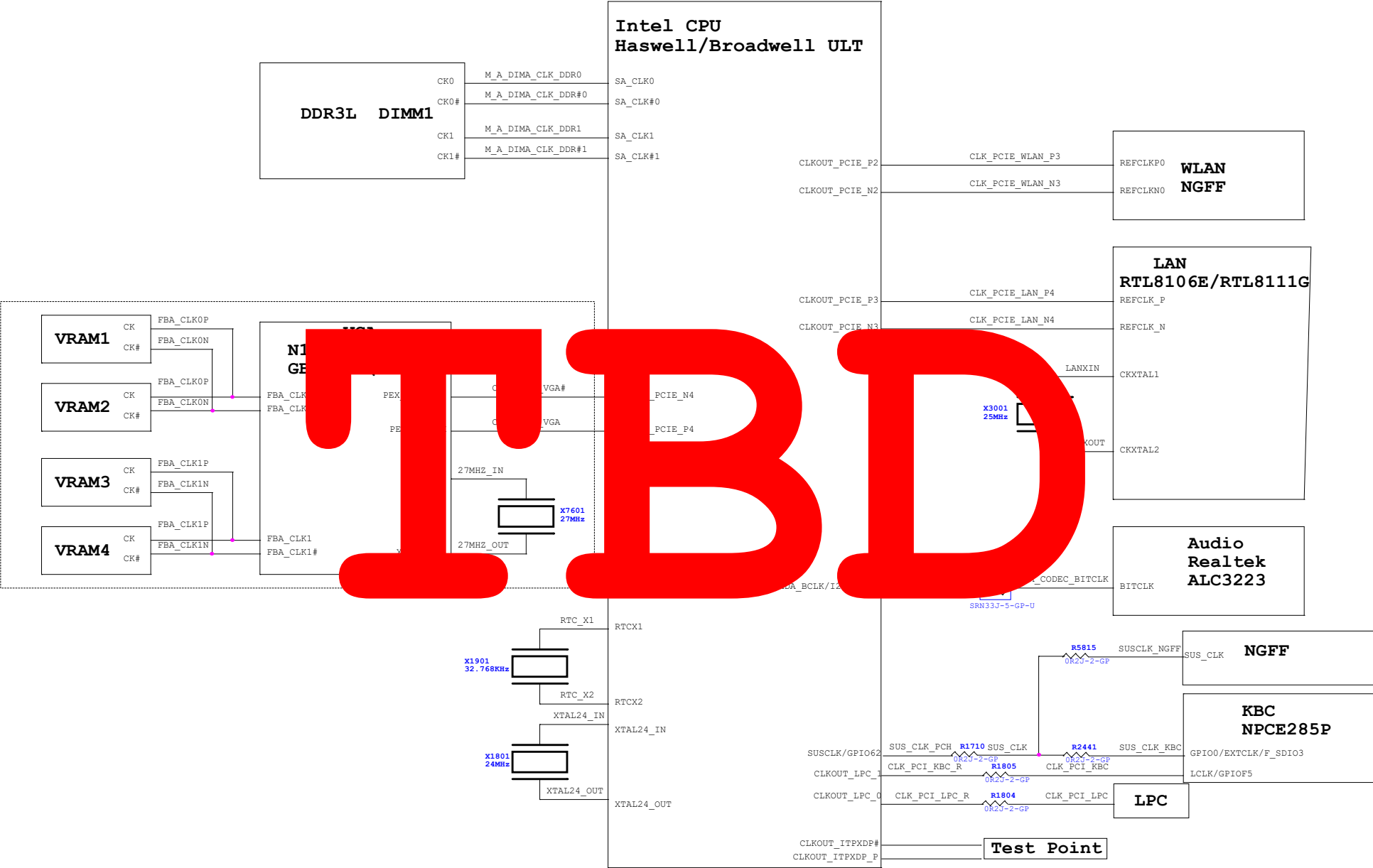
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Commercial (Firmware SW)			
Size	Document Number	Rev	
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follow KyloRen 13 2017-06-12

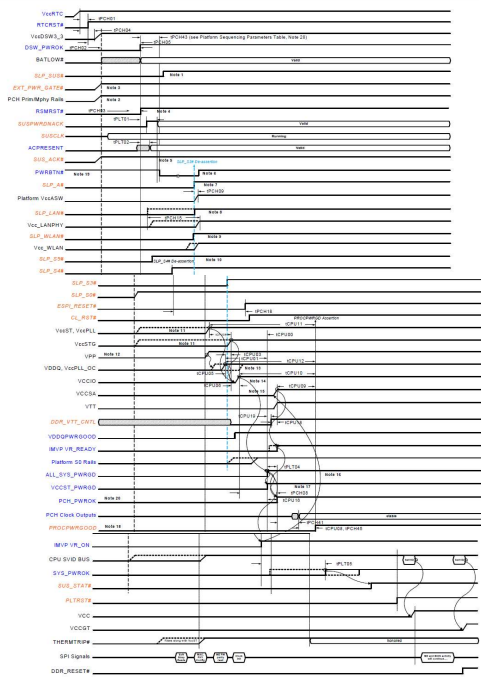


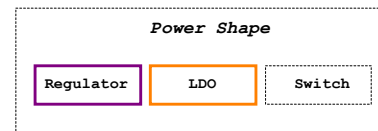
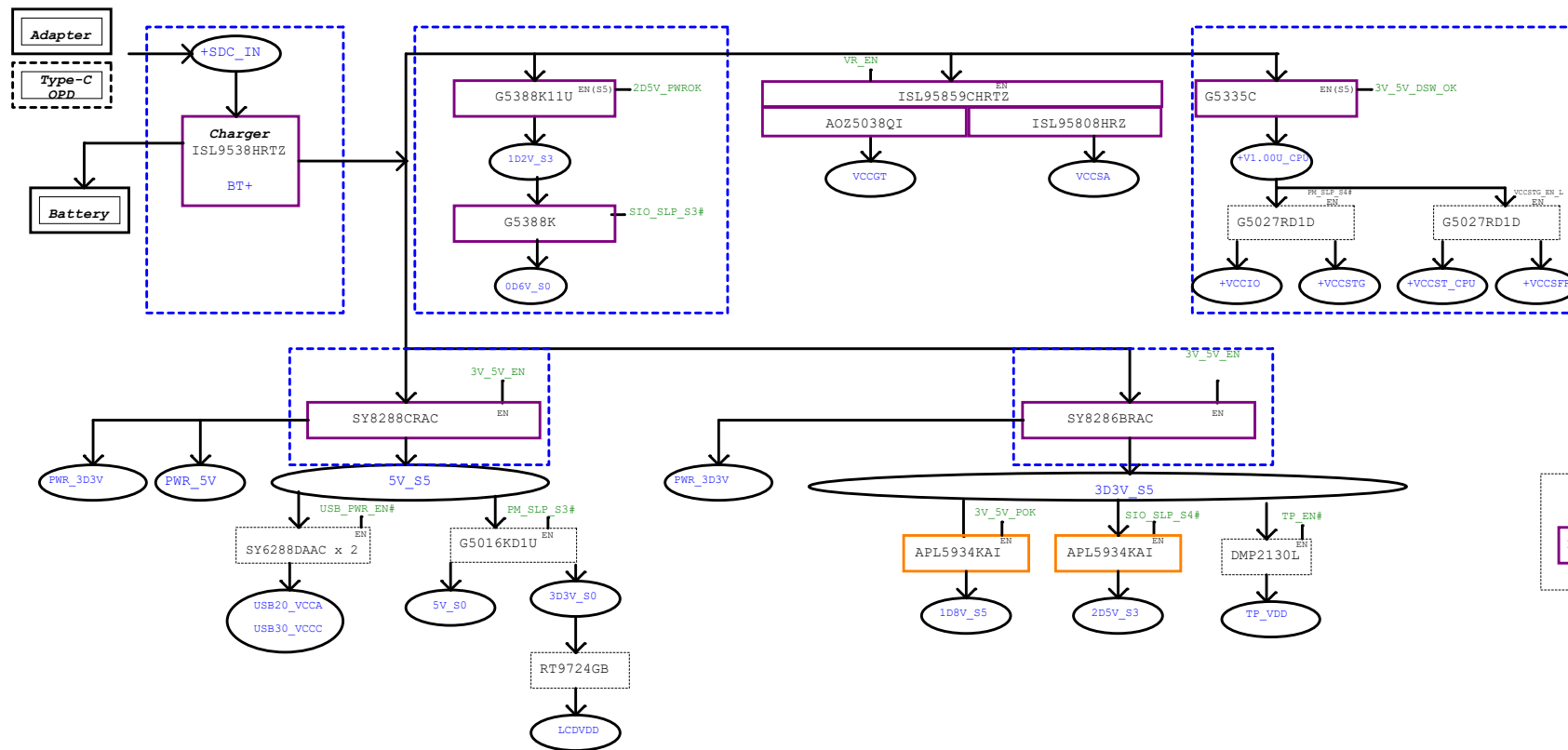
CLK Block Diagram



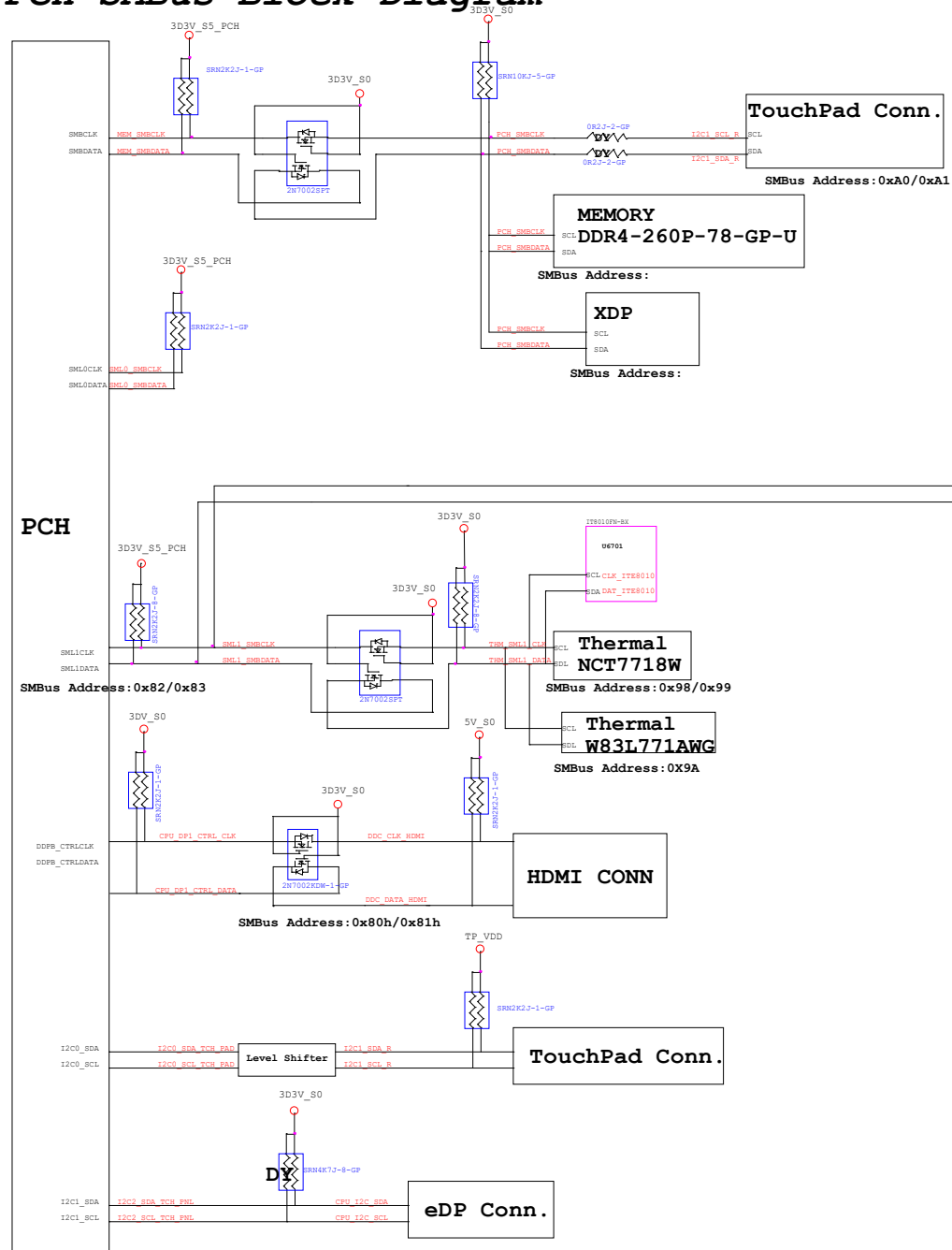
[illegible][illegible]

For DDR4 power sequence

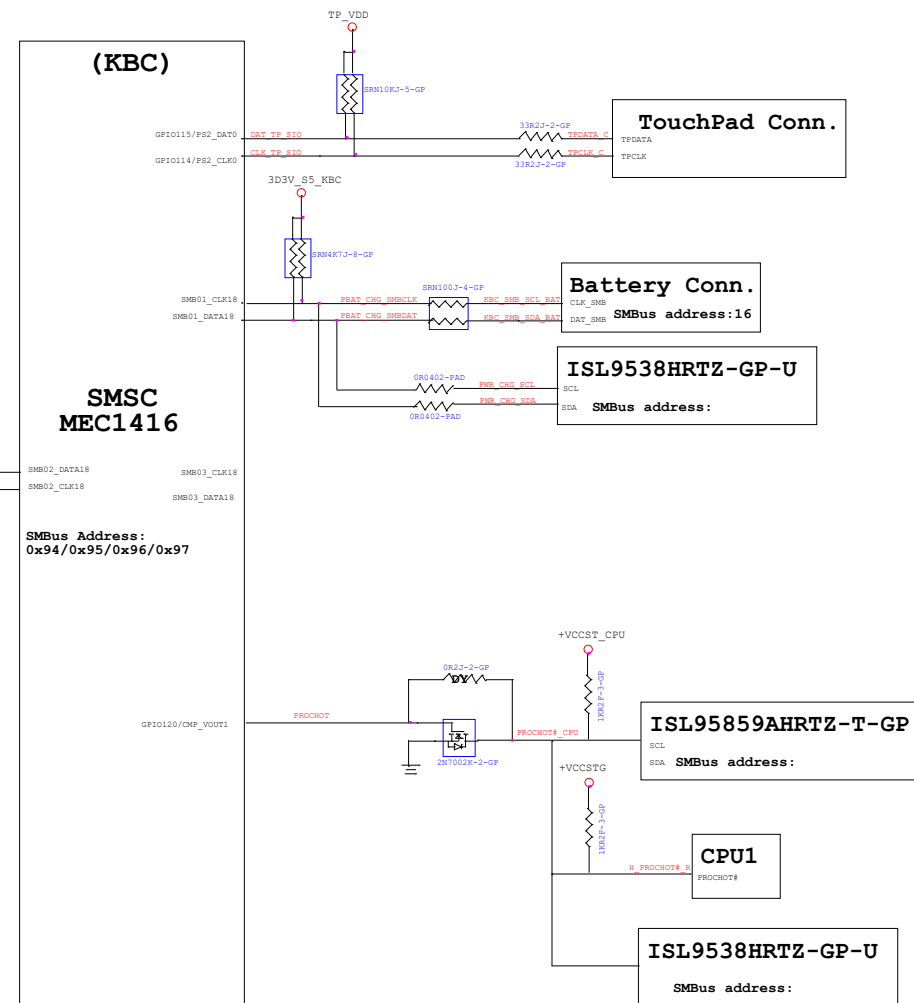




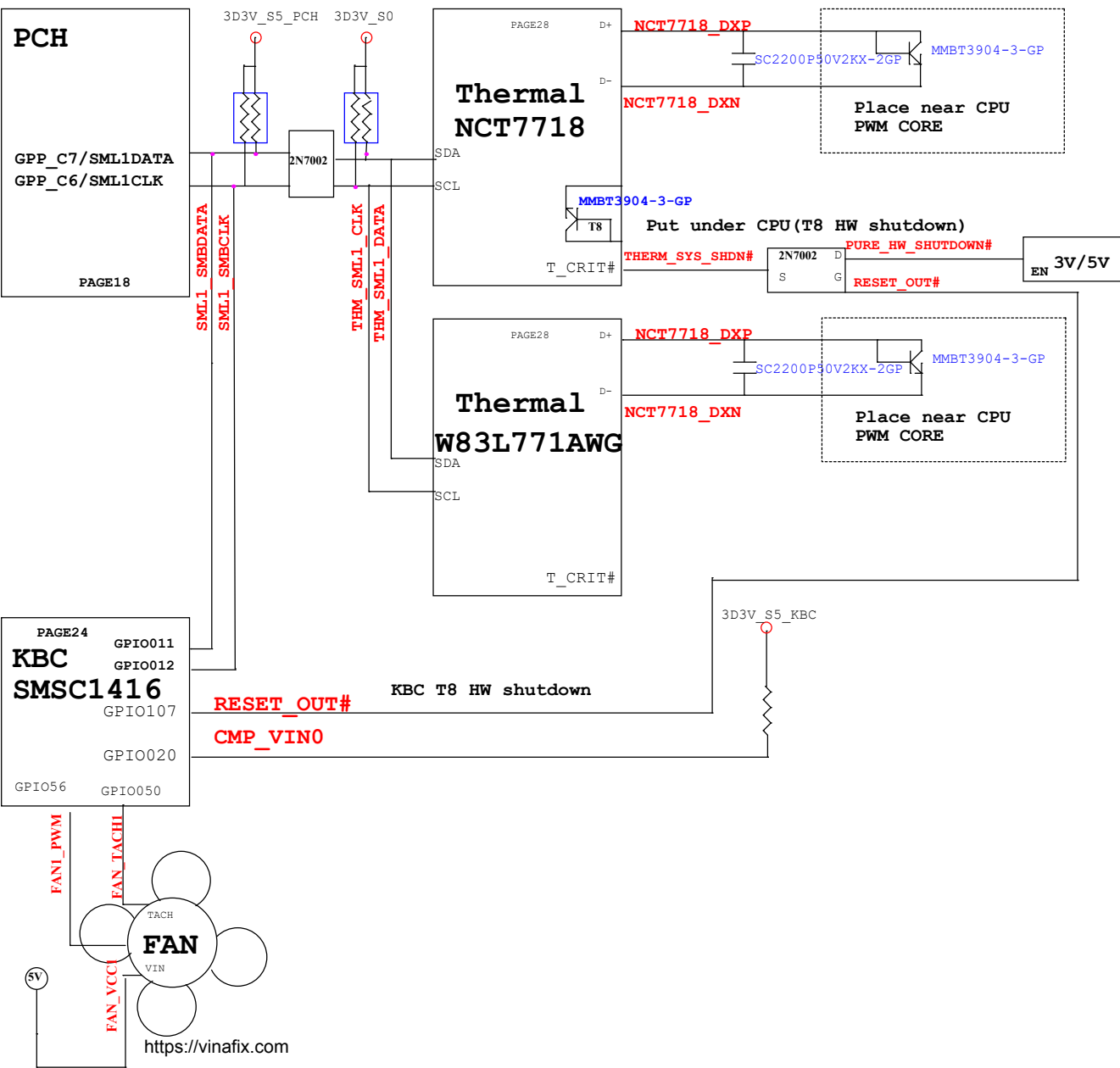
PCH SMBus Block Diagram



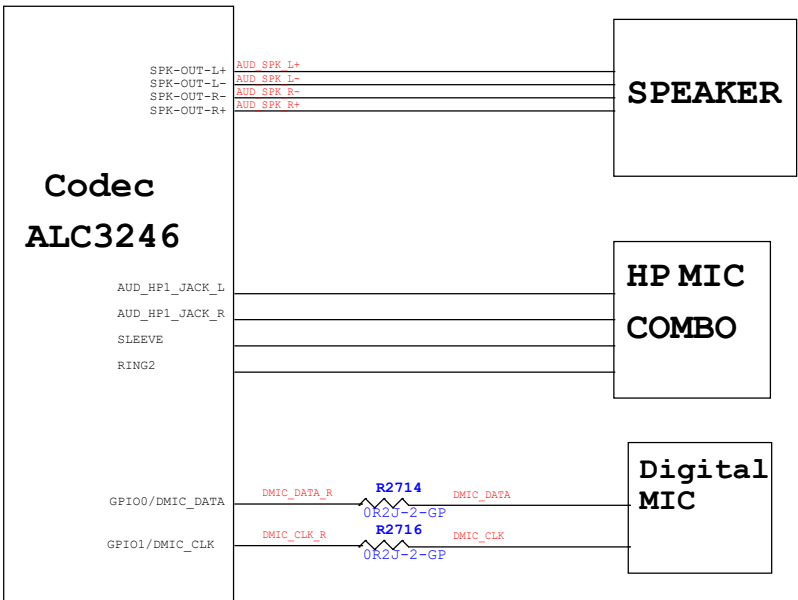
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Pinehills		CPU				Function
PWA	Architecture	Celeron	Pentium	SMB i3	Core i5	Type-c
1	Kaby Lake U	v				
2	Kaby Lake U		v			v
3	Kaby Lake U			v		v
4	Kaby Lake R				v	v

MB P/N	CPU description	CPU P/N	TYPE-C
455.0FN01.D001	Celeron DC	5W00F	No
455.0FN01.D002	i3 SMB0	9THWP	Yes (Conn. DEREN)
455.0FN01.D003	i5	15GR7	Yes (Conn. FOXCONN)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

CLK Block

Size
A

Document Number

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